Bulletin CW 809-2

# Interface Integrated Circuits Lesson Summaries

# INTERFACE INTEGRATED CIRCUITS

## COURSE LESSON SUMMARY

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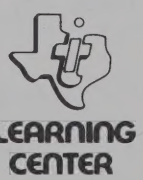
For use only in conjunction with the Texas Instruments Interface Integrated Circuits videotape course.

**Prepared by Texas Instruments Learning Center**

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# INTERFACE INTEGRATED CIRCUITS
## COURSE LESSON SUMMARY

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# ABOUT THE AUTHORS

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**Don L. Cannon, PhD.** Serves on the staff of Texas Instruments Learning Center. Assistant Professor, University of Texas at Arlington, Electrical Engineering Department. Industrial experience in thin film and semiconductor microelectronics. Also device physics, reliability and computer-aided design.

**Gerald Luecke, MSEE.** Texas Instruments Learning Center. Manager, Advanced Technology Educational Programs. Associated with integrated circuits since 1960 leading to advanced work in TTL, ECL and MOS ICs. Broad experience in monolithic and hybrid circuitry including semiconductor memories. Holds several patents and has authored numerous articles and papers on solid-state circuit design and applications.

**Jack P. Mize, PhD.** Serves as Staff Consultant to Texas Instruments Learning Center. Former Associate Professor of Electronic Sciences at SMU. Previously, associated with TI directing R&D projects on discrete semiconductors and integrated circuits including MOS/LSI technology.

**John A. Mooney, BSEE.** Senior Design Engineer, Electro-Optics Division, Equipment Group, Texas Instruments. Design experience: Circuit and equipment design for optical detectors and infrared data processing. His special emphasis has been low-noise, direct-coupled amplifier design and applications.

**Robert A. Stehlin, MSEE.** Heads IC Design Center of Advanced Components in the Semiconductor Research and Development Laboratory, Texas Instruments. Has held design responsibility for MOS/LSI ramdom-access memory using enhancement mode and depletion-mode MOS transistors as well as bipolar circuits using complementary transistor structure. Program manager for radiation-hardened linear and bipolar IC design and fabrication.

# TIPS ON GETTING THE MOST FROM THIS COURSE

You've had at least 16 years of education so we won't presume to teach you how to learn. But chances are that very few of your courses were on videotape – and videotape requires some minor modifications in your classroom habits.

**Listen fast and watch fast.** Videotaped lectures typically cover four times as much material as a live professor does in the same length of time. With a live prof, you have plenty of time to probe for errors in what he's just said, or to envision applications, or to sit and contemplate, while he sketches a schematic, or looks up a reference, or talks about the Super Bowl game. But the efficiency of videotape cuts out all these time wasters, and gives you a highly concentrated message. If you sneeze, you'll miss something important. If the lecture raises any question in your mind, jot it down so you can get a clarification after the tape, but put it out of your mind while you absorb the rest of the lecture.

**Relax.** Nobody's going to interrupt the TV lecturer with questions, and he's not going to ask you for opinions. You can count on being free from such distractions, so you can free your consciousness to absorb the material like a sponge.

**Take very few notes.** This Course Lesson Summary contains every figure you'll see on the screen including formulas and related information. The Summary is also a record, in print, of the speaker's remarks. Limit your notes to brief comments that will help you study later – write them where they belong in the Summary, so they'll be handy.

It is suggested that you not try to follow the speaker's words in the Summary as they are significantly abbreviated into good note form to help reduce your distraction from the specific points that the speaker is emphasizing.

**Enjoy it.** Engineering education via videotape is the wave of the future, brought to you today. Over the years, attendees at videotaped seminars from TI's Learning Center have found them to be not only informative and an optimal use of their time, but enjoyable as well. We hope you do, too.

# TV CLASSROOM ARRANGEMENT

The success of a videotape course depends greatly on one simple but critical factor – how well the students can see the screen.

These recommendations are based on studies by G. F. McVey, PhD, University of Wisconsin.

All dimensions that are expressed in feet are based on the typical 23″ diagonal screen, but are accurate to ±3′ for 17″ and 25″ screens.

All measurements are to students' **eyes**, not knees or shoulders.

1. Seat no one closer than 7′ from screen.

2. Seat no one further than 20′ from screen.

3. Seat no one more than 30° off perpendicular to screen. (Roughly, not more than 4′ off center, 7′ back; not more than 10′ off center, 20′ back.)

4. For small audiences, cluster seats around "Best Seat in the House," indicated on Figure 1.

5. Allow 30″ width for each student, whether you're using "theatre" seating or "classroom" seating.

6. If you're using "theatre" seating (no tables), allow 32″ **depth** between chair backs.

7. If you're using "classroom" seating (using tables, which we recommend), allow 30″ **plus** depth of table, between chair backs as indicated on Figure 2.

8. Use tables not more than 20″ deep, if at all possible. (Good hotels have them.)

9. Orient tables and chairs to face screen straight on. (Keeping the neck turned is fatiguing.)

10. Keep room at **normal light level**, not dark. (A dark room lets the pupil of the eye dilate, degrading focus and introducing aberrations.)

# TV CLASSROOM ARRANGEMENT (CONTINUED)

11. Close draperies to exclude bright sunlight.

12. Face the audience away from windows.

13. Seat yourself near the main door, in position to intercept visitors and minimize distractions.

14. Allow at least 2′ of unobstructed walking space all the way around the audience.

15. If you have more than 33 people, you need another monitor.

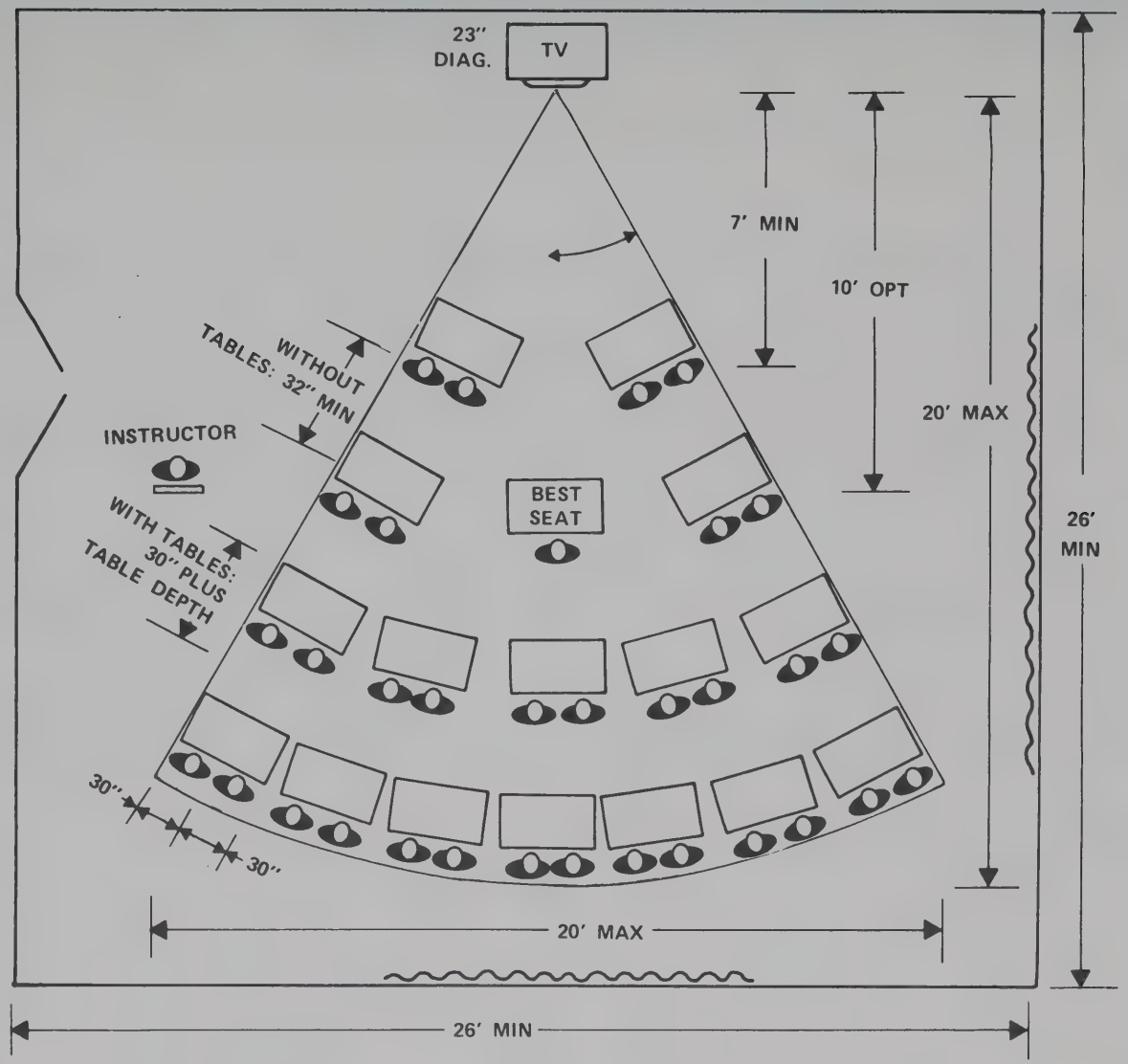


Figure 1. Seating Arrangement for Less Than 33 Students

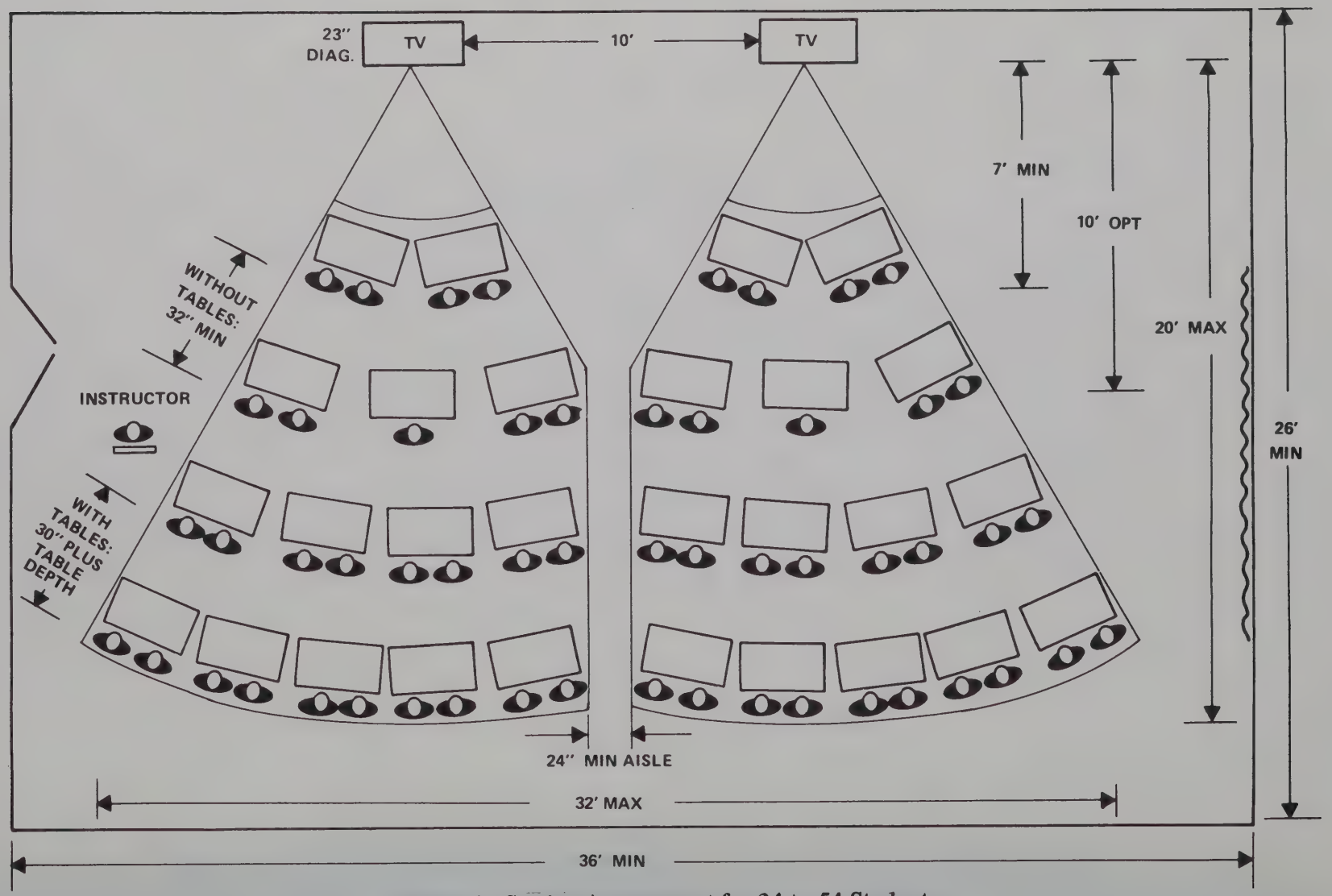


Figure 2. Seating Arrangement for 34 to 54 Students

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# Lesson 1

# LINEAR IC TECHNOLOGY-I

*General overall technology considerations for all linear ICs including the types of devices commonly used, their structures and their characteristics.*

# Lesson 1

# LINEAR IC TECHNOLOGY-I

*General, overall technology considerations for all linear ICs are covered in this session. There is another session, "Linear IC Technology – II," that supplements this session for the designer interested in more details.*

*A quick review of the information of an N-P-N transistor in a typical integrated circuit is provided by the next series of figures.*

**Beginning of an N-P-N Transistor** **(Figure 1.1)**

The "general" IC begins with a slice of p-type silicon. Then using standard planar photo-masking and diffusion, a heavily doped n region, called an "n-plus" region, is produced. Its purpose is to improve the conductivity of the collector region of the transistor.

**Epitaxial Layer** **(Figure 1.2)**

A layer of lightly doped n-type silicon is grown over the entire surface of the slice, using epitaxial techniques. Then a p-diffusion is made down through the epitaxial layer to contact the p-type substrate. This leaves an n-region and the associated n-plus region entirely surrounded by p-type material. This is the "isolation" diffusion. It produces an n-type region.

**Base and Emitter Diffusions** **(Figure 1.3)**

First, a p-type base region is diffused. Then a heavy n-plus diffusion is made for two purposes: first, on the right, for the n-type emitter region; and second, on the left, for a high-conductivity point for the collector region.

**Metallization** **(Figure 1.4)**

Finally, the aluminum film is evaporated onto the final oxide layer with metal extending down through windows to contact the collector region, the base region, and the emitter region. This produces a "vertical" N-P-N transistor.

The voltage breakdown and saturation parameters of the transistor are determined by the thickness and resistivity of the epitaxial layer which is the collector region.

The first n-plus diffusion, under the epitaxial film, is used to carry current from the lightly doped collector region to the vicinity of the collector contact. The saturation characteristics are thus improved without sacrificing breakdown voltage.

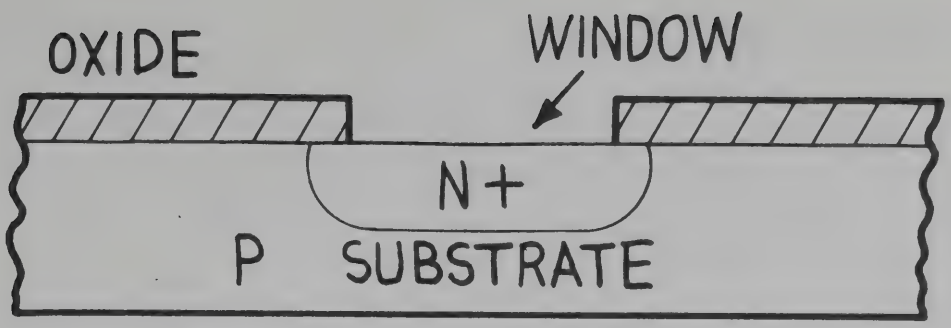



Figure 1.1. Beginning of an N-P-N Transistor

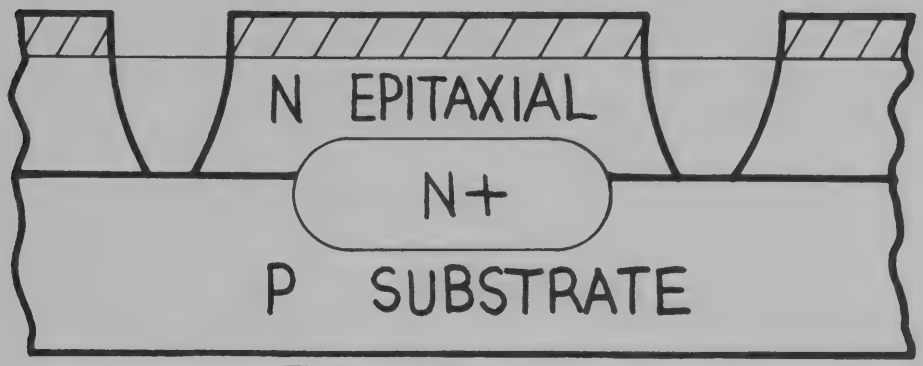



Figure 1.2. Epitaxial Layer

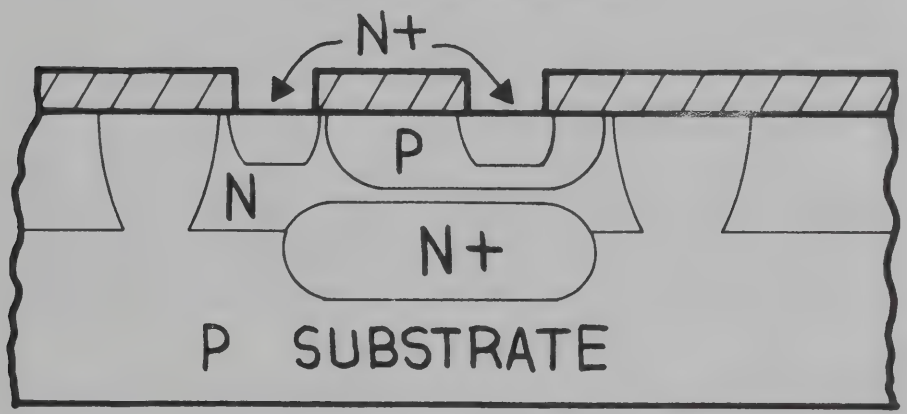



Figure 1.3. Base and Emitter Diffusions

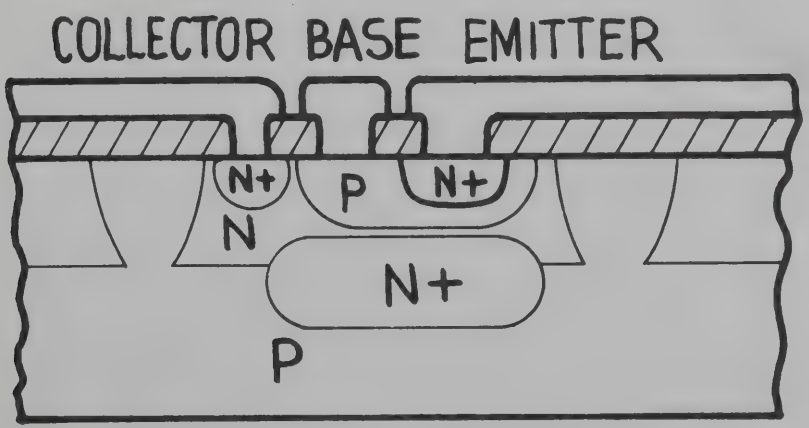



Figure 1.4. Metallization

**Input Impedance of an Op Amp** **(Figure 1.5)**

The circuit of a typical differential input section for an op amp is shown in this figure. The input impedance is just twice the $h_{ie}$ of the two transistors. But $h_{ie}$ depends on the beta of the transistors. Obviously then, when the beta is degraded by gold doping, the very critical input impedance of the op amp is also degraded. Op amps are not normally gold doped due to the loss of $h_{fe}$ for P-N-P devices.

**Diffused Resistor** **(Figure 1.6)**

This figure shows a perspective drawing of a conceptual cross section of one resistor, without the oxide or the metallization. Within the n-region is a relatively long and narrow strip of p-region that was formed at the same time as the base of the vertical N-P-N transistor. This strip is the diffused resistor. Metal contacts are attached to each end of the strip.

**Resistance of Diffused Resistor** **(Figure 1.7)**

The resistance value of this resistor depends on the dimensions and on the average resistivity of the material.

The actual design of a diffused resistor is simplified by utilizing the concept of sheet resistance, $R_S$. This is the average resistivity divided by the junction depth.

**Temperature Curves for Diffused Resistors** **(Figure 1.8)**

This figure shows some measured temperature curves for two typical p-type diffused resistors. One has sheet resistance of 100 ohms per square; the other has 200 ohms per square. The temperature characteristics are a strong function of sheet resistance. Sheet resistance is simply the average resistivity divided by the depth of the resistor diffusion.

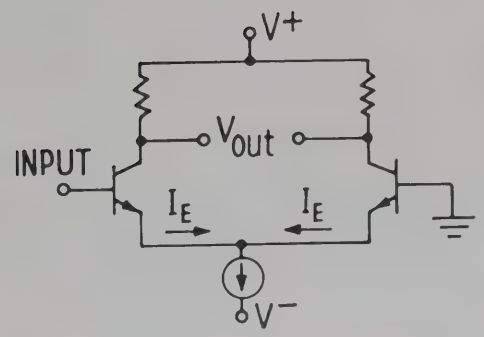



Figure 1.5. Input Impedance of an Op Amp

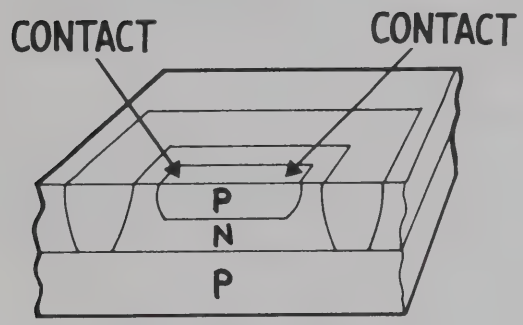



Figure 1.6. Diffused Resistor

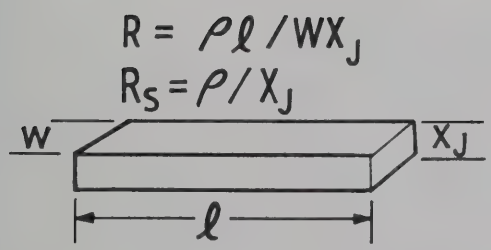



Figure 1.7. Resistance of Diffused Resistor

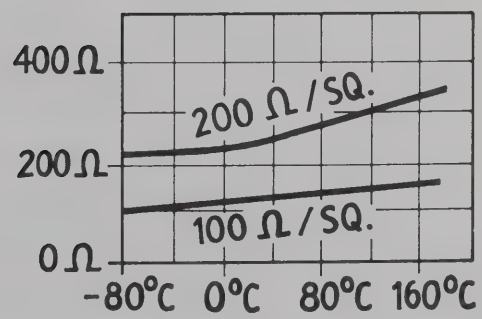



Figure 1.8. Temperature Curves for Diffused Resistors

**MOS Capacitor** **(Figure 1.9)**

A conceptual cross section of an MOS capacitor is shown in the figure. As with the resistor structure, the semiconductor regions here are created by utilizing some of the same steps required to form the vertical N-P-N transistor.

The n-plus region is contacted over the right edge by a metallized lead on top of the oxide film. The oxide is shown over the n-plus region as being thinner than elsewhere. Oxide thicknesses in various regions will vary according to how many diffusions have been made in each region.

Finally, a metallization region is formed on top of the oxide that covers the n-plus region. Thus the MOS capacitor is formed by the metal over the n-plus region, with the oxide as a dielectric and the n-plus region as the lower plate.

Another way a capacitor is made in an IC, of course, is by using a reverse-biased diode junction. However, the MOS type of capacitor has several distinct advantages. First, it is nonpolar. Second, there is little or no voltage modulation of capacitance. Third, the Q is normally higher, due to lower parasitic capacitance.

**Internal Compensation of an Op Amp** **(Figure 1.10)**

This is the type 741 internally compensated op amp. The 30-picofarad capacitor is at a high-impedance node. Its function is to provide a continuous rolloff of six decibels per octave, so that no external compensation is required.

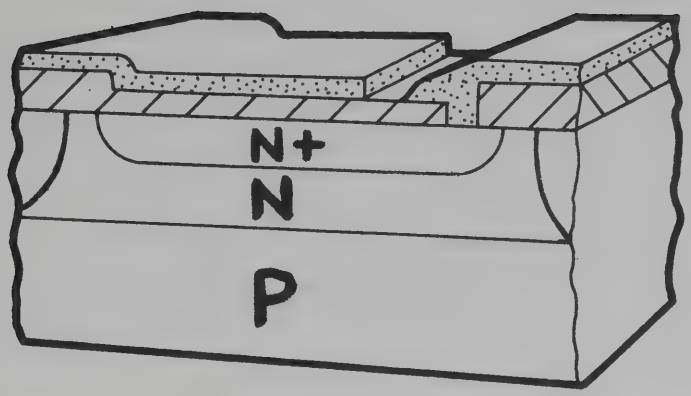



Figure 1.9. MOS Capacitor

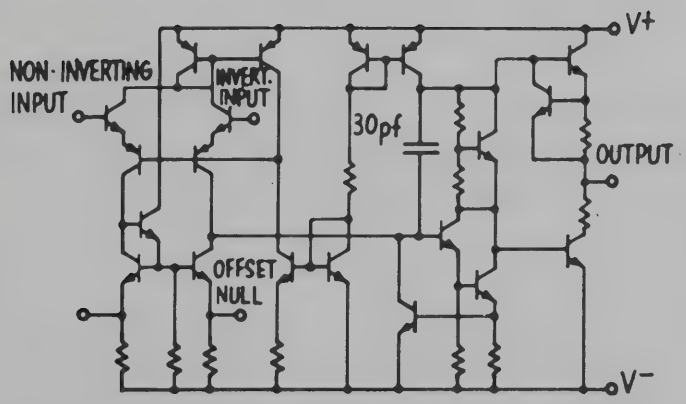



Figure 1.10. Internal Compensation of an Op Amp

**Type 741 IC Chip** **(Figure 1.11)**

This figure is a photograph of a Type 741 IC chip. It measures about 50 by 50 mil. The 30-picofarad MOS capacitor takes up a great deal of the chip area. MOS capacitors therefore are used only sparingly in integrated circuits.

Linear integrated circuits in production today rarely resemble the conventional designs. The main reason for the difference is that discrete designs utilize a greater variety of components. These include inductors, large capacitors, large resistors, precision resistors, and resistors with low temperature coefficients. The components are simply not available in integrated form.

However, close matching of both active and passive devices over a wide temperature range, and excellent thermal coupling throughout the circuit, can be obtained with integrated circuits.

Active devices in integrated form are more economical then passive components. Additionally, new devices that have no exact counterpart among readily available discrete devices are provided by IC technology. These include lateral P-N-P transistors with multiple collector segments, the Schottky-barrier-diode-clamped transistor, and others.

The rest of this session is devoted to some of the less ordinary IC components. First, the lateral P-N-P transistor is considered.

**Lateral P-N-P Transistor** **(Figure 1.12)**

The oxide and metallization are not shown in the figure. The four diffusions can be seen clearly. The isolated n-region serves as the base of the P-N-P, with two n-plus regions for good conductivity. The p-type emitter and collector regions are formed by the N-P-N base diffusion, with the collector encircling the emitter.

The current gain of lateral P-N-Ps ranges from 5 to 100. The breakdown voltage of the emitter-base junction is just as high as that of the collector-base junction, which makes this device attractive for input stages that require high input breakdown voltage.

**Active Load** **(Figure 1.13)**

In this figure a P-N-P is supplied with a constant base current. It is used in the place of a large resistor as the load for the N-P-N transistor. The P-N-P active load is used to produce high-voltage gains without the excessive chip area that would be required by a diffused resistor of equivalent value.

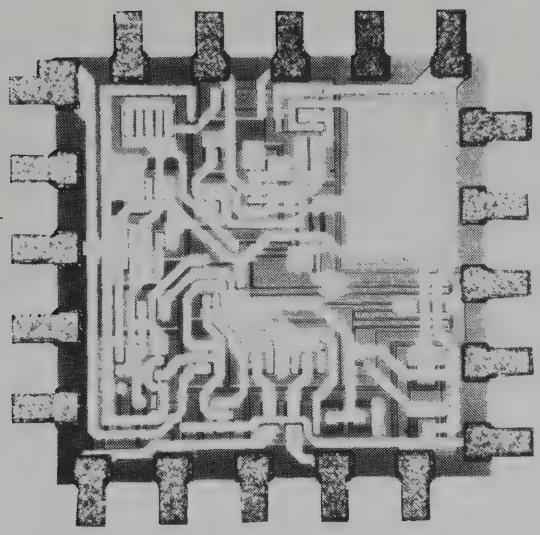


Figure 1.11. Type 741 IC Chip

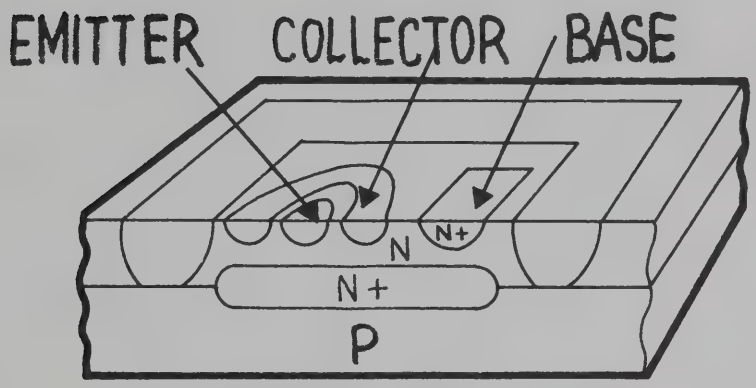



Figure 1.12. Lateral P-N-P Transistor

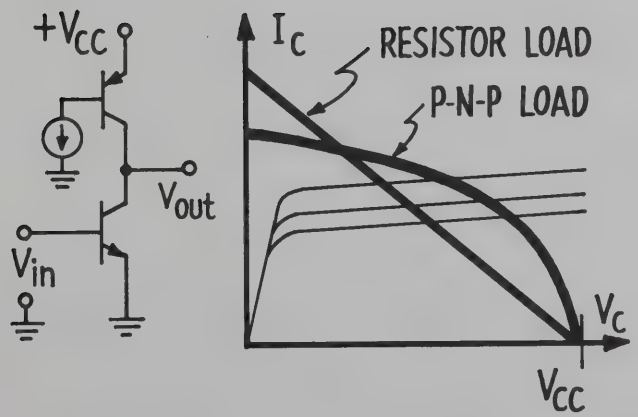



Figure 1.13. Active Load

**Modified Lateral P-N-P Transistor** **(Figure 1.14)**

A conceptual top view of the modified P-N-P transistor shown at the left. The shaded circle represents the emitter diffusion. The collector ring is shown broken into two segments, with areas denoted $A_C$ standing for the effective collector area, and $A_F$ representing feedback collector area.

The symbol for this multisegment collector is shown at the right. The useful feature of this structure is that the current gain is set by the design of the surface geometry of the collector diffusion. Very precise control of the gain is thus achieved.

The effective beta, which is $I_C$ divided by $I_B$ is approximately equal to the ratio of the areas of the two collector segments, $A_C$ over $A_F$.

**Application of Lateral P-N-P Transistors** **(Figure 1.15)**

An application of multisegment P-N-Ps is shown in this figure. It is the input stage of the Type 101A op amp. Lateral P-N-P transistors Q3 and Q4 are biased through a common constant current source. By using split collectors, the gain of these P-N-Ps is controlled to less than five.

The high base-emitter breakdown voltage of the lateral P-N-Ps here allows differential input voltages equal to the power supply voltage, without damage.

The lateral P-N-P does have a limitation with regard to small-signal frequency response. The device has excessive phase shift at frequencies above about two megahertz, so it is limited to low-frequency circuits.

**Super-Beta Transistor** **(Figure 1.16)**

A super-beta transistor has the same configuration as a standard vertical N-P-N, as shown in this figure. However, before the standard emitter diffusion step, a special emitter diffusion is made for all super-beta devices on the slice. The result is a deeper emitter than normal, with a correspondingly more narrow base width or thickness. A thin base region means high beta and low collector-emitter breakdown voltage.

The result is an order-of-magnitude improvement in the input current and impedance specifications for an op amp.

**Application of Super-Beta Transistors** **(Figure 1.17)**

This figure shows a voltage-follower design. Super-beta transistors are used in the input stage to set very low input bias current. The diode is included to operate Q2 at a collector-base voltage near zero. For the same reason, the collector of Q1 is bootstrapped to the output. Therefore, low-voltage transistors can be used in the input. The only transistor to see any appreciable voltage is Q3, which buffers the output.

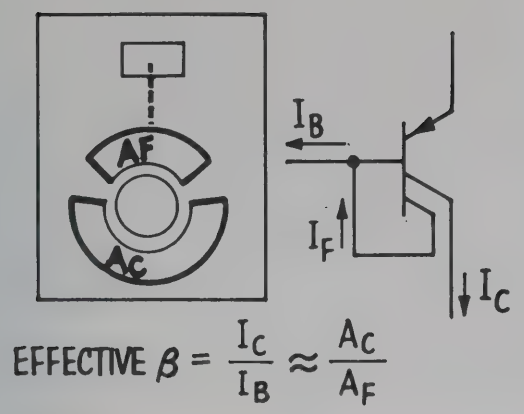



Figure 1.14. Modified Lateral P-N-P Transistor

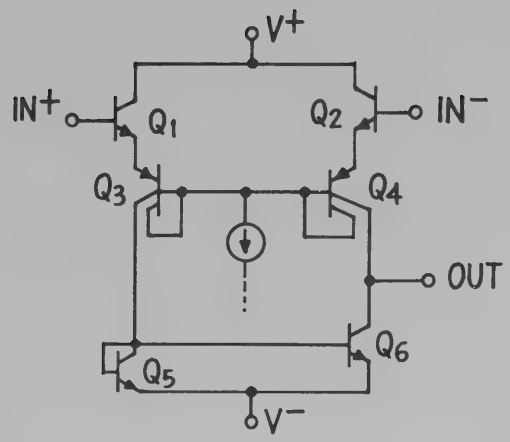



Figure 1.15. Application of Lateral P-N-P Transistors

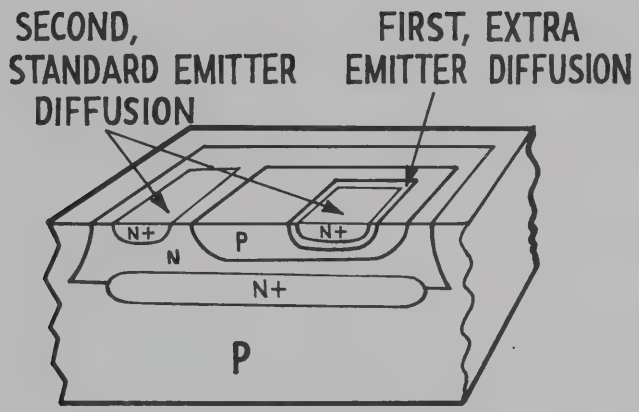



Figure 1.16. Super-Beta Transistor

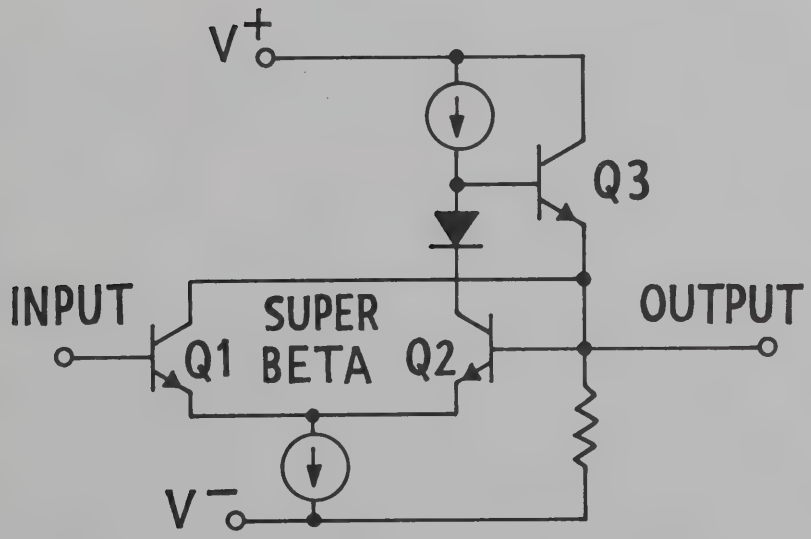



Figure 1.17. Application of Super-Beta Transistors

**Schottky-Clamp Method of Improving Speed** **(Figure 1.18)**

To improve the switching speed of a vertical N-P-N transistor in a comparator, a Schottky-barrier diode is simply built into its structure, connected in parallel with the base-collector junction. The switching time of Schottky-barrier diodes is extremely fast, as there are no minority carriers to store up charge in the diode structure. Also, the forward voltage is only about three tenths of a volt. The purpose of the diode is to clamp the base to the collector, and thus prevent the transistor from ever going into full saturation.

**Symbol for Schottky-Clamped Transistor** **(Figure 1.19)**

The generally accepted symbol for a Schottky-clamped transistor is shown in the figure.

**Schottky-Clamp Structure** **(Figure 1.20)**

Concept of the Schottky-clamp structure is shown in the figure. A slightly enlarged base contact metallization is formed at the top with the darker base diffusion below, the emitter at the left, and the collector region further down. To make the Schottky diode, a hole is simply left through the base diffusion. The junction of the base metallization with the lightly doped collector region forms the contact-barrier Schottky diode between the collector and the base. As a result, the turn-off time is greatly reduced.

## SUMMARY

Standard components such as the vertical N-P-N transistor, diffused resistor, and diodes are used in linear integrated circuits. Additionally, MOS capacitors, lateral P-N-P transistors, super-beta transistors, and Schottky-clamped transistors are frequently used.

All of these components are formed by the same four diffusion steps, except that the super-beta transistor requires one extra diffusion before the last standard one.

Although linear IC designers are faced with more limitations than discrete linear circuit designers, IC technology provides certain additional, unique advantages that more than make up for the deficiencies. In this manner, linear IC technology is meeting the demands of today's advanced systems.

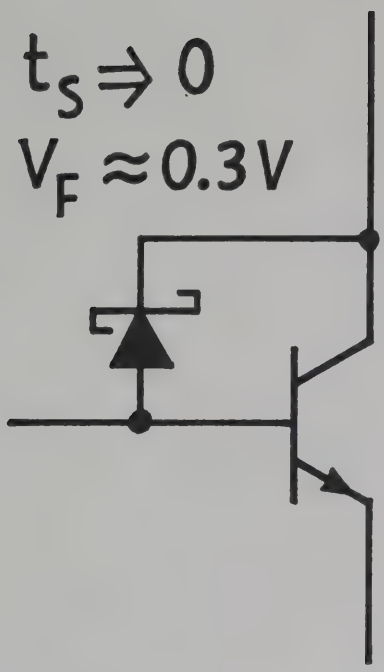



Figure 1.18. Schottky-Clamped Method of Improving Speed

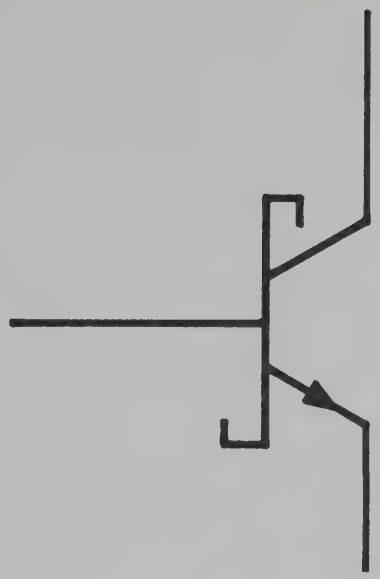


Figure 1.19. Symbol for Schottky-Clamped Transistor

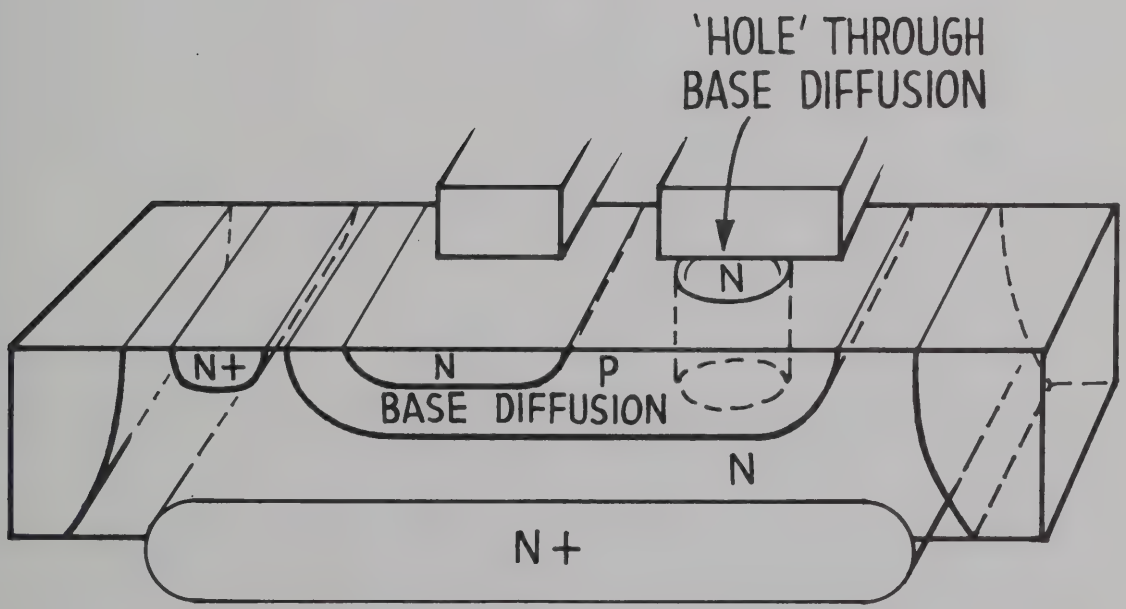



Figure 1.20. Schottky Clamp Structure

# Lesson 2

# LINEAR IC TECHNOLOGY-II

*An additional technology session to provide background for the application of linear and interface integrated circuits. It includes an extension of the first session for common devices, includes more exotic devices such as FETs, current source structures for complementary devices.*

# Lesson 2

# LINEAR IC TECHNOLOGY-II

*This lesson will first complete the survey of devices that are used fairly commonly in present-day linear ICs by looking at several kinds of resistors other than the diffused variety. Then several circuit design techniques will be covered that are illustrative of the unique methods to which linear IC designers must resort.*

**Pinch Resistor** **(Figure 2.1)**

There are some specialized resistor techniques used in linear ICs. This is a conceptual cross section of the "pinch resistor" structure. The oxide and metallization layers are not shown to allow the observation of the top of the chip. There is an isolated portion of the n-type epitaxial layer and within it is a p-type diffused resistor. At the rear is one of the contact points for the resistor.

There is a section of n-plus emitter diffusion over the mid-section of the resistor. This n-plus region is similar to a field effect transistor gate and the p-type resistor diffusion acts as an FET channel. In operation, a reverse bias is maintained on the "gate-channel" junction, causing a constriction of the effective cross section of the diffused resistor in a sort of "pinching" action, hence, the name "pinch resistor."

This FET structure is not operated in the "pinch-off" region and is not used as an FET in the sense of an active device, as no signal is applied to the so-called "gate." This merely raises the sheet resistance of the resistor to around 10 to 30 kΩ per square, giving a high-value resistor in a relatively small area.

**Pinch Voltage-Current Plot** **(Figure 2.2)**

The characteristics of pinch resistors are not linear over the usable voltage range. This is a typical V-I plot that shows this fact. These curves are for a "gate source" voltage of zero and for three different temperatures. Note the rather low breakdown voltage – around 6 to 8 volts – due to the heavily doped gate. The device has a strong positive temperature coefficient on the order of 3000 to 5000 ppm/°C.

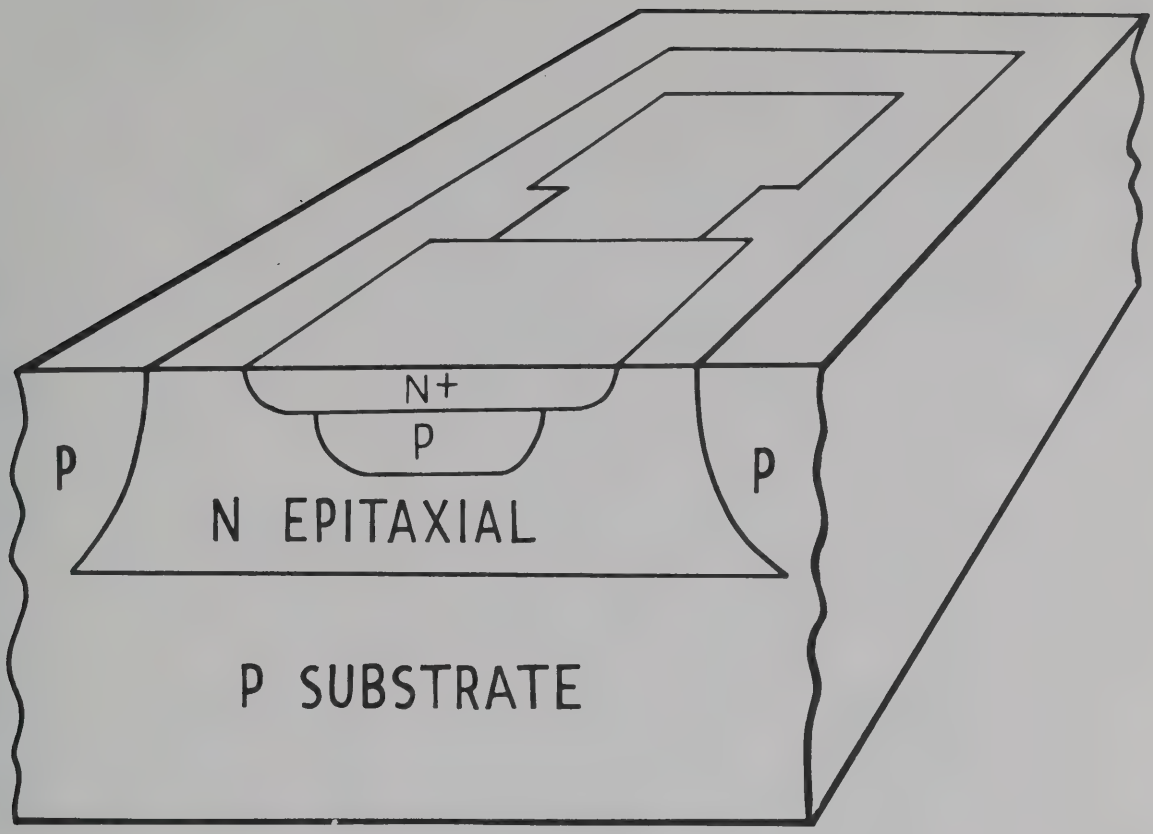



Figure 2.1. Pinch Resistor

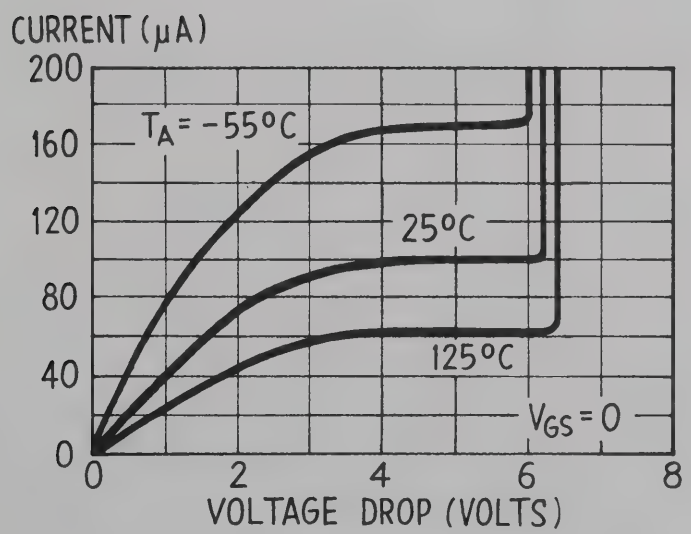



Figure 2.2. Pinch Voltage-Current Plot

**101A Op Amp** **(Figure 2.3)**

Absolute values of the pinch resistor are difficult to control. This device is valuable for uses, such as a bleed resistor, where the breakdown and tolerance problems do not affect the circuit performance. As an example, consider this input stage of the Type 101A op amp. The input has two transistors and a pinch resistor. This configuration improves the input offset voltage and the large-signal frequency response. The 40 kΩ resistor here acts in an emitter-base "bleeding" capacity; and it can be a pinch resistor, since its absolute value and temperature coefficient are not critical to circuit performance. The matching and tracking of pinch resistor structures on the same chip can be held to within plus or minus five percent.

**Collector FET Resistor** **(Figure 2.4)**

The second technique for achieving a high-value resistor in a small area is called the "collector FET." This is a drawing of this concept. The collector FET is in effect a simplified pinch resistor, using an isolated strip of n-type epitaxial material as the "channel," rather than having a separately diffused p-type channel.

The mid-section of the expitaxial strip is "roofed over" by a p-type N-P-N base diffusion. The name "collector" FET comes from the fact that the expitaxial region is normally used as the collector for N-P-N transistors. The chief advantage of the collector FET over the pinch resistor is its higher breakdown voltage. This structure offers a sheet resistance of 2 to 10 kΩ per square. The use of this device is restricted somewhat, due to the fact that the gate is connected to the most negative point in the circuit, the substrate. This collector FET type of resistor has been effectively used in circuits where the operating biases are determined by current sources as shown.

**Collector FET Application** **(Figure 2.5)**

This collector FET is providing a very large resistance, about 300 Ω, in a small area. The FET resistor can be connected directly across the power supply, allowing a wide range of operating voltages.

**Zener Diode Level Shifting** **(Figure 2.6)**

Because of the limitations imposed on designers by integration techniques, the designers have evolved some rather unique methods differing from traditional discrete circuit configurations. In discrete design, direct coupling of successive stages is typically done with complementary N-P-N and P-N-P transistors. However, in most monolithic circuits, P-N-P transistors are not readily available with the exception of the rather limited lateral P-N-P. Consequently, new methods had to be developed. One possible option is shown here. The base-emitter junction of a transistor can be used as a zener diode for level shifting. However, the range of zener voltages is restricted by the base process to a value between 5.4 and 8.0 volts. Furthermore, zener diodes tend to introduce excessive noise into the circuit.

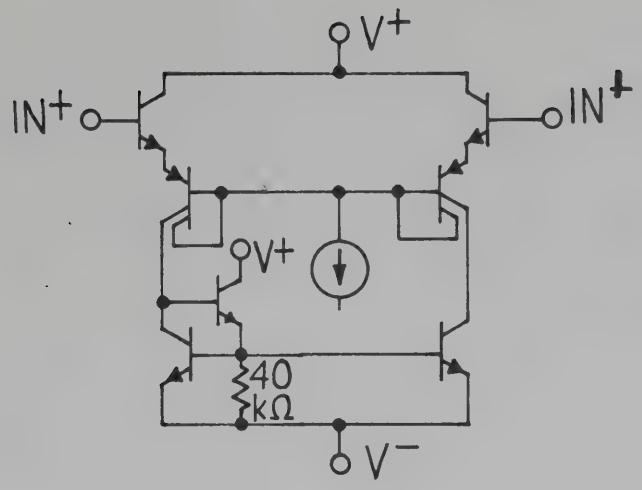



Figure 2.3. 101 A Op Amp

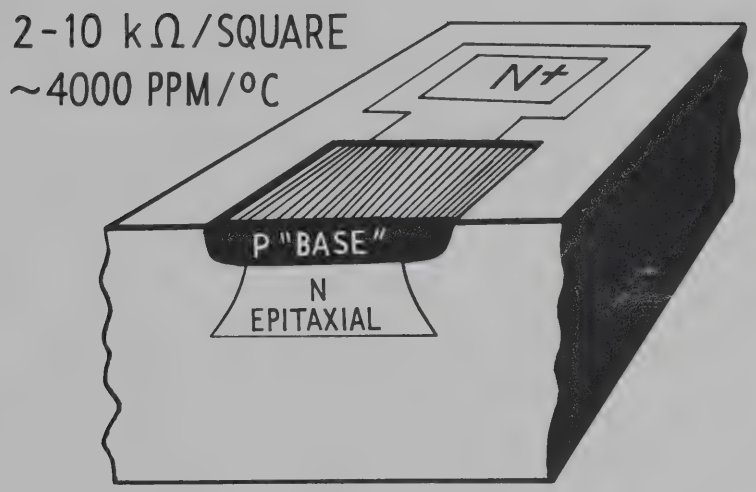



Figure 2.4. Collector FET Resistor

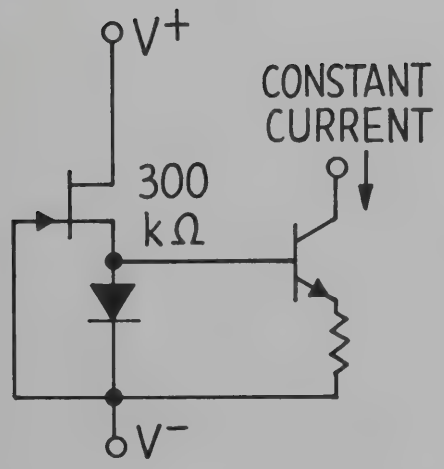



Figure 2.5. Collector FET Application

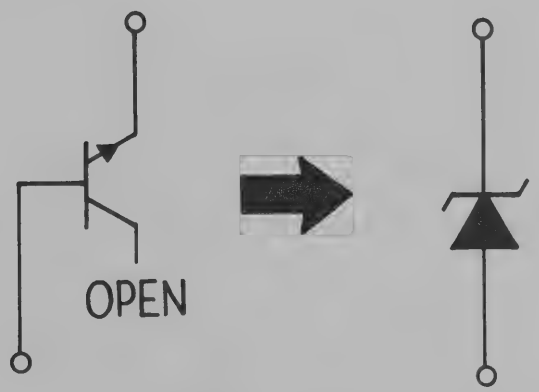



Figure 2.6. Zener Diode Level Shifting

**Series Resistor Level Shifting** **(Figure 2.7)**

In this level-shifting circuit, the transistor is an emitter-follower stage. Due to the constant current source, the dc voltage level is shifted as shown by this formula.

This circuit suffers from process variations because $R_1$ may vary as much as 20% from chip to chip. However, a significant modification will take care of this tolerance problem.

**Transistor Resistor-Divider Level Shifting** **(Figure 2.8)**

With the resistor divider and second transistor in the place of the resistor, the level shift is now as shown in this figure. The matching of resistor ratios is one of the strong points of integrated circuits; however, both these circuits have large temperature coefficients.

**Diode Biased Transistor Current Source** **(Figure 2.9)**

ICs have the advantage of close matching of identical components on the same chip. This fact is used to advantage in forming constant current sources. The simplest form of current source is called the diode-biased transistor as shown. This configuration is called diode biased because Q1 has its base and collector shorted together. Q1 is not a diode but a truly active device. Q1 and Q2 are constructed identically so their characteristics match very closely. And, since the base of Q2 is connected to the base of Q1, the two collector currents need to be identical.

**Small Current Constant Current Source** **(Figure 2.10)**

By varying the area of these two emitters, the ratio of the two collector currents can be made to vary. The upper equation relates the emitter areas to the current ratios. A simple modification of the diode-biased circuit will give a constant current of extremely small value. Just add a small-value resistor in the emitter circuit of Q2 and change the equation for $I_2$. This resistor introduces a difference between the base-emitter voltages of the two transistors, shown as $\Delta V_{BE}$. This gives the transcendental logarithmic relationship between $I_2$ and $I_1$. This configuration is relatively insensitive to variations in $I_1$ due to the logarithmic factor in the equation.

**Feedback Loop Constant Current Source** **(Figure 2.11)**

This figure illustrates an improvement on the basic constant current source. There is a diode-connected transistor, Q1, on the right, and two identical resistors R1 in both emitter circuits. The additiional transistor Q3 forms a feedback loop. The main point of this is that the base currents of Q3 and of Q2 are very nearly equal, so they cancel each other out and the feedback loop compensates for changes in $h_{FE}$.

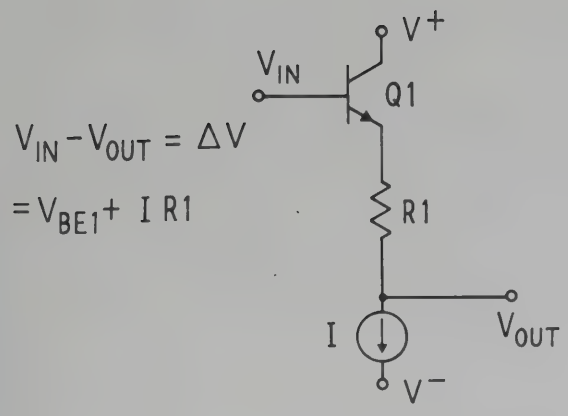



Figure 2.7. Series Resistor Level Shifting

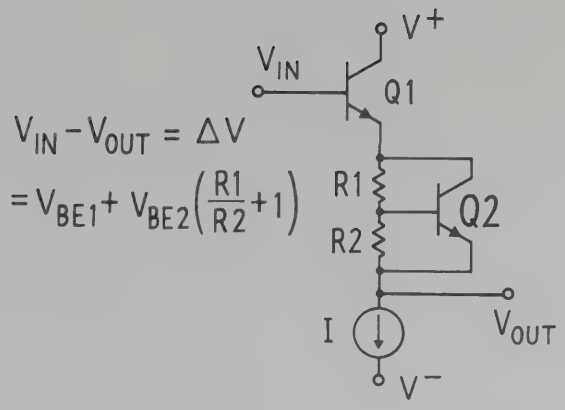



Figure 2.8 Transistor Resistor-Divider Level Shifting

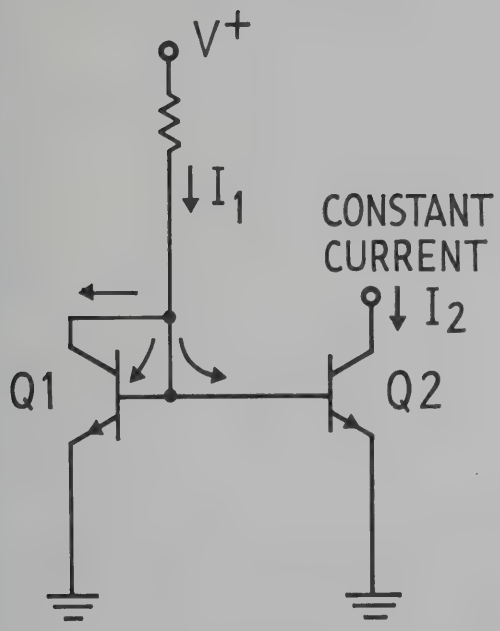



Figure 2.9. Diode Biased Transistor Current Source

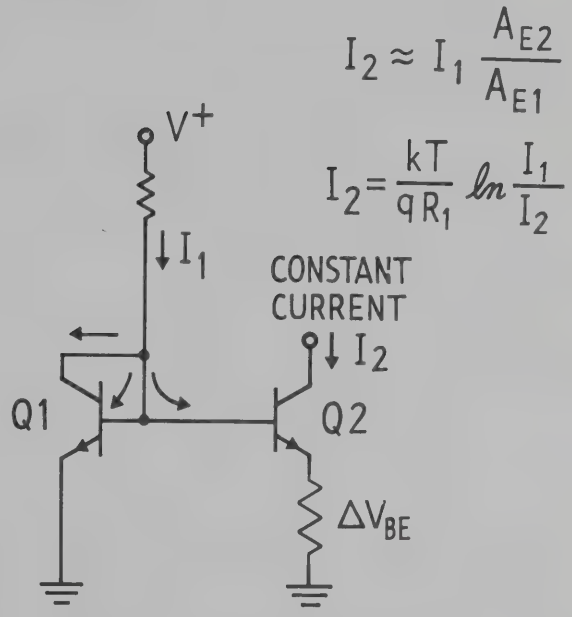



Figure 2.10. Small Current Constant Current Source

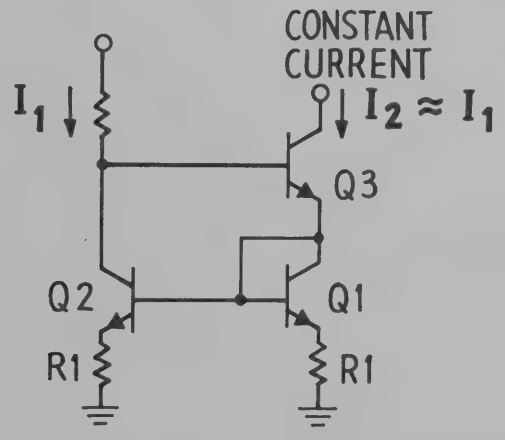



Figure 2.11. Feedback Loop Constant Current Source

**Step One of Dielectric Isolation** **(Figure 2.12)**

There are some newer aspects of linear IC technolgoy that are unusual. One concerns dielectric isolation, meaning the separation of integrated circuit elements from each other by a film of dielectric, usually silicon dioxide, rather than by the tranditional reverse-biased semiconductor junction. Besides being used for "radiation hardening," this is an excellent way to reduce parasitic effects between the individual devices and the substrate. To achieve dielectric isolation, start with an n-type substrate and grow an n-plus epitaxial film as shown.

**Step Two of Dielectric Isolation** **(Figure 2.13)**

The next step is to etch grooves with well-defined angular walls down through the epitaxial film, and then grow an oxide layer. There is now a separate little pedestal or island for each individual device that is to be formed.

**Step Three of Dielectric Isolation** **(Figure 2.14)**

The next step is to deposit a very thick layer of polycrystalline silicon on top of the oxide film, using an epitaxial technique.

**Step Four of Dielectric Isolation** **(Figure 2.15)**

The substrate is then lapped away by a grinding process until a slight amount of the polycrystalline upper layer has been exposed. Then the slice is inverted, and the effective substrate is the polycrystalline layer. At the surface are pockets of monocrystalline silicon isolated by the dielectric oxide film. From this point on, normal integrated circuit processing is used to complete the fabrication.

**Photograph of IC Chip Using Dielectric Isolation** **(Figure 2.16)**

The isolation films are two oxide strips, with polycrystalline silicon between. This dielectric isolation process is coming into fashion to improve the high-frequency performance of linear ICs.

**Conventional Integrated N-P-N Parasitic Elements** **(Figure 2.17)**

To understand how and why the performance of dielectrically isolated circuits differs from that of conventional ICs, examine this equivalent schematic of the parasitic elements inherent in a conventional integrated N-P-N transistor. This is a four-layer N-P-N-P structure comprising the emitter, base, collector, and substrate. The N-P-N transistor desired is shown in bold lines; the parasitic elements are lighter. Parasitic elements such as these are a part of every device in a conventional IC chip, and they constitute a serious limitation of circuit performance.

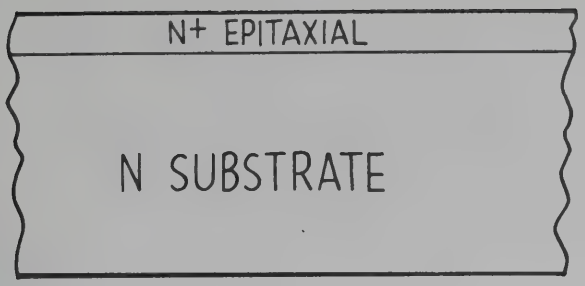



Figure 2.12. Step One of Dielectric Isolation

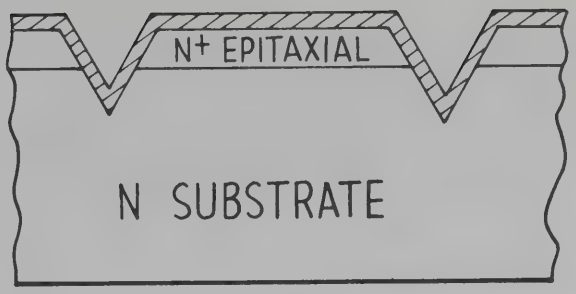



Figure 2.13. Step Two of Dielectric Isolation

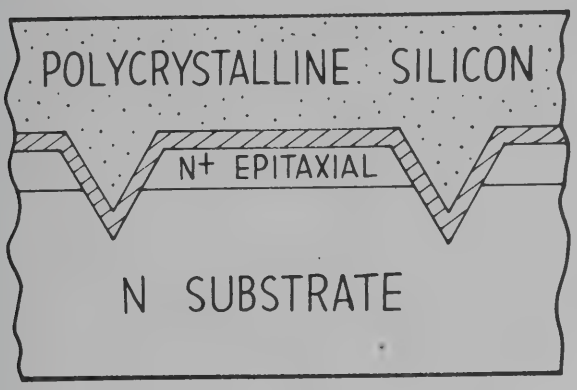



Figure 2.14. Step Three of Dielectric Isolation


Figure 2.15. Step Four of Dielectric Isolation

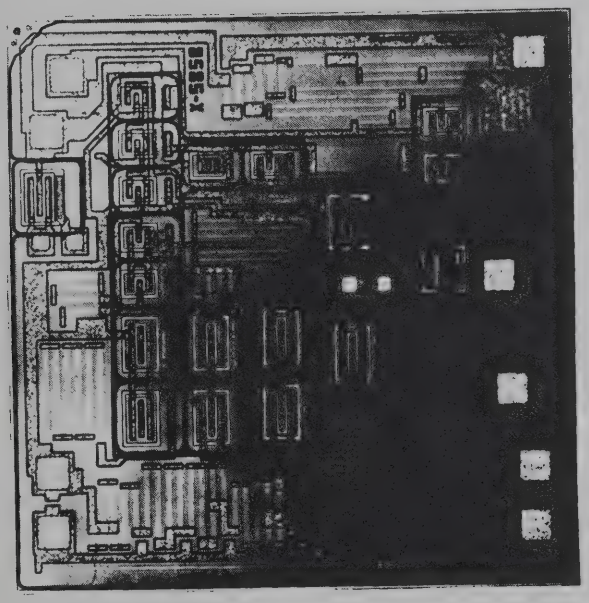


Figure 2.16. Photograph of IC Chip Using Dielectric Isolation

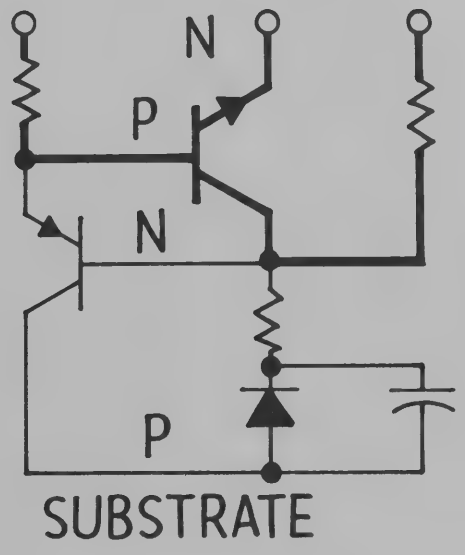



Figure 2.17. Conventional Integrated N-P-N Parasitic Elements

**Dielectrically Isolated Parasitic Elements** **(Figure 2.18)**

The parasitic effects encountered with dielectrically isolated components are much fewer and weaker. This is an equivalent circuit of an N-P-N transistor of this type. The structure is not N-P-N-P, but N-P-N oxide, with a polycrystalline substrate. If leakage through the oxide is ignored the substrate parasitics consist only of a very small capacitance with a series resistance.

**Vertical P-N-P for Linear ICs** **(Figure 2.19)**

Another reason for using dielectric isolation in linear ICs is to create vertical P-N-P transistors which are very close complements of vertical N-P-N devices. This complementary structure is shown here. On the left is a dielectrically isolated P-N-P transistor; and on the right, for comparison purposes, is an N-P-N device. The n-plus epitaxial layer was omitted and a p-region was diffused for the P-N-P collector before etching the isolation grooves. To create the n-type base and the p-plus regions, two additional diffusions are required.

**Dielectrically Isolated Complementary Pair** **(Figure 2.20)**

This figure is a typical application of a dielectrically isolated complementary pair in the output stage of an operational amplifier. The direct-coupled complementary output, operating in a push-pull manner, gives high output currents, increased frequency response, and high efficiency.

**Dielectrically Isolated Differential Amplifier** **(Figure 2.21)**

A more interesting application of the P-N-P is shown in this figure. This is an amplifier stage that provides over 60 dB of voltage gain. The input transistors Q1 and Q2 form a basic differential amplifier. The "loads" of the differential amplifier are the P-N-P transistors Q3 and Q4. The single-ended output is formed by the collectors of Q1 and Q4. The input stage has a common-mode input range of approximately the full power-supply swing.

**Linear IC J-FET** **(Figure 2.22)**

A linear IC technology even newer than dielectric isolation is the use of junction FET or J-FET in the input stages of amplifiers. The J-FET can provide wider bandwidths and greater slewing rates than super-beta transistors. Here is a typical structure for a p-channel J-FET used in linear ICs. A special high-resistivity p-diffusion forms the FET channel, with source and drain contacts to be made at either end. A standard n-plus emitter diffusion across the channel acts as the top gate region.

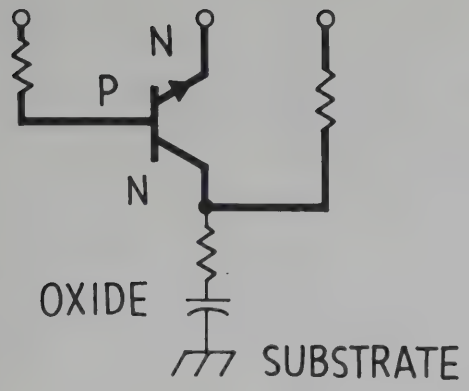



Figure 2.18. Dielectrically Isolated Parasitic Elements

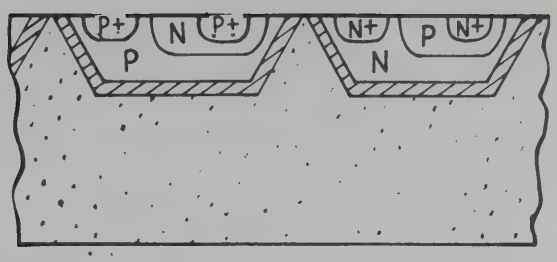



Figure 2.19. Vertical P-N-P for Linear ICs

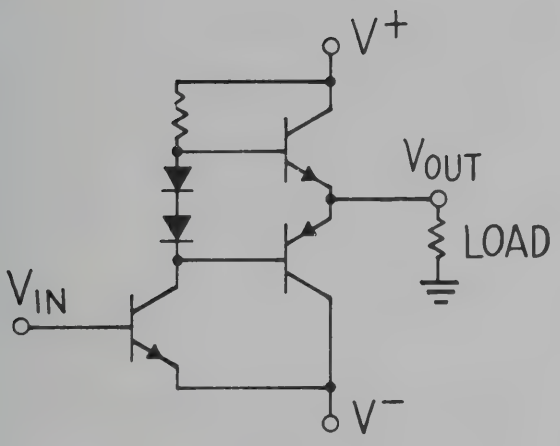



Figure 2.20. Dielectrically Isolated Complementary Pair

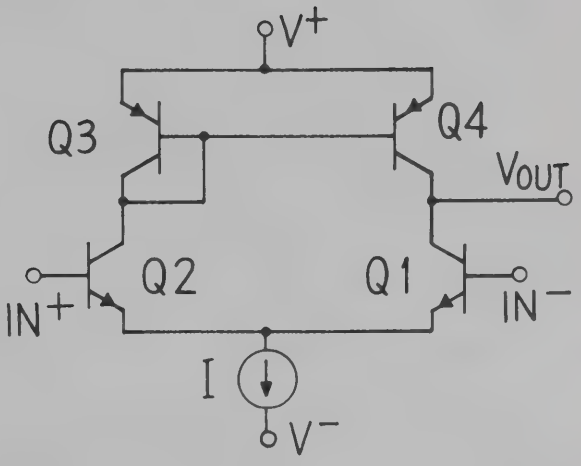



Figure 2.21. Dielectrically Isolated Differential Amplifier

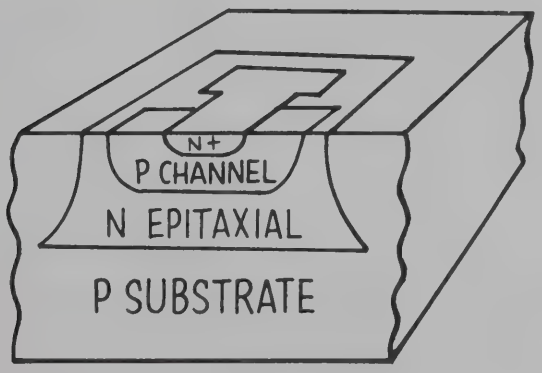



Figure 2.22. Linear IC J-FET

**J-FET Input Stage** **(Figure 2.23)**

This is a typical J-FET input stage for an op amp. The two J-FETs are used to obtain input currents of less than 0.1 nanoamp. J-FETs can also be used in the current source, giving a high impedance to increase the common-mode rejection.

**N-Channel J-FET Structure** **(Figure 2.24)**

This structure is sometimes used for n-channel J-FETs in linear ICs, without requiring any additional diffusion steps as the p-channel device does. The isolated epitaxial region forms the channel, and the standard p-type base diffusion is used for the top gate. The substrate forms the bottom gate, which does limit the application of this structure.

**Linear IC MOSFET** **(Figure 2.25)**

The next logical step in the progression toward lower and lower input currents is the use of MOS FETs in linear ICs. However, putting MOS and bipolar transistors on the same chip entails an additional processing step that is rather critical, namely, the thinning of oxide under the MOS gates. It does appear that MOS FETs are destined for eventual use in linear ICs, because they could give input impedances as high as $10^{16}$ ohms. This figure shows the concept of the most likely MOS FET structure that would be used in linear ICs. This is a p-channel enhancement-type structure akin to that commonly used in digital MOS ICs. The standard bipolar base diffusion is used to form the source and drain regions within an isolated n-region that extends over to the left to be grounded. The oxide film is shown and, over it, the metallization.

**MOS FET Linear Input Stage** **(Figure 2.26)**

A possible MOS input stage for a linear circuit is shown here. Typical MOS op amps presently have low gain, high input offset voltage, and noisy inputs, but very high input impedance. The zener diodes are required for protecting the very thin gate oxide from breakdown.

**Low-Input Leakage MOS-Input Amplifier** **(Figure 2.27)**

A particularly attractive application for a low-input leakage MOS-input amplifier is a sample-and-hold circuit with input information intermittently stored on the capacitor via the MOS switch and read out continuously at the right.

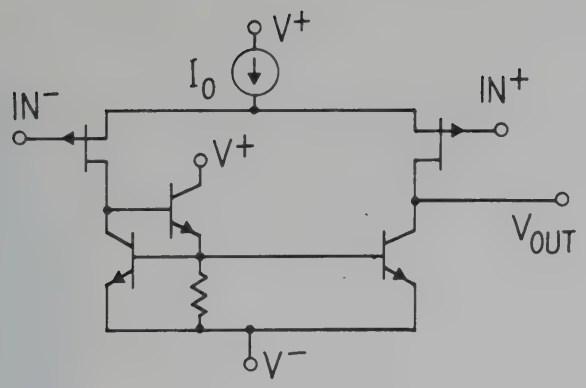



Figure 2.23. J-FET Input Stage

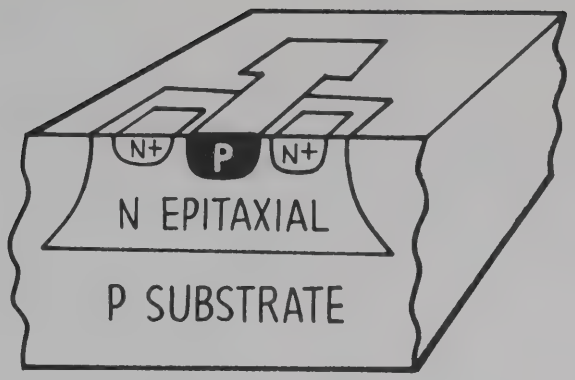



Figure 2.24. N-Channel J-FET Structure

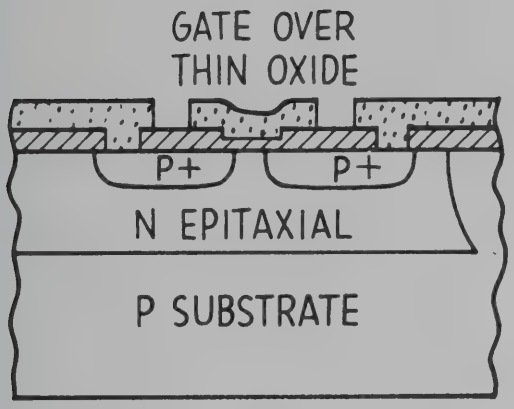



Figure 2.25. Linear IC MOSFET

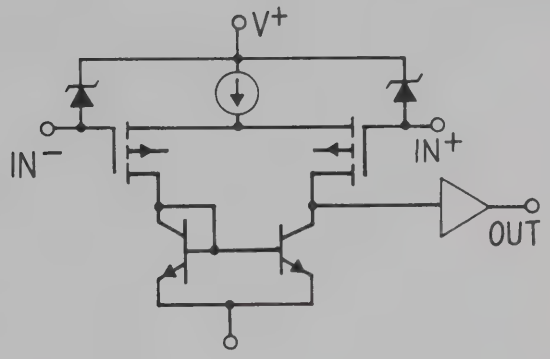



Figure 2.26. MOSFET Linear Input Stage

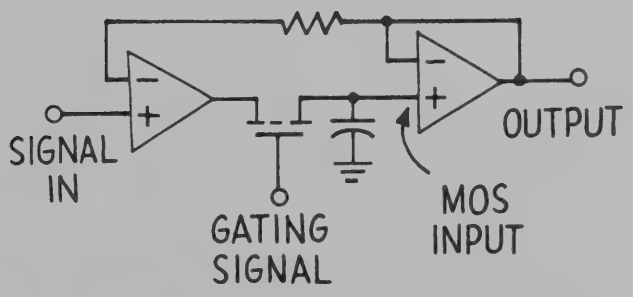



Figure 2.27. Low-Input Leakage MOS Input Amplifier

**Total MOS Amplifier** **(Figure 2.28)**

One last linear MOS circuit to consider is shown here. This is a total MOS amplifier. The two loads and the current source are depletion-mode MOS FETs rather than enhancement-mode like the others. These are formed by ion implantation of boron across the channel region of these particular devices on the chip, a process that is also used in digital MOS ICs.

## SUMMARY

This lesson has been intended to give a feel for the limitations imposed on linear circuit designers by the basic structure of integrated circuitry. There are many unique device structures and circuit configurations used by linear IC designers to overcome the handicaps of integration and create new circuit functions that were never feasible before. Beyond this knowledge of present-day linear ICs, this lesson has discussed some of the probable future directions of the technology; trends toward better performance involving the use of dielectric isolation, junction FETs, and even MOS FETs. Perhaps the most important fact to keep in mind is that linear IC technology is continually evolving and the best is yet to come.

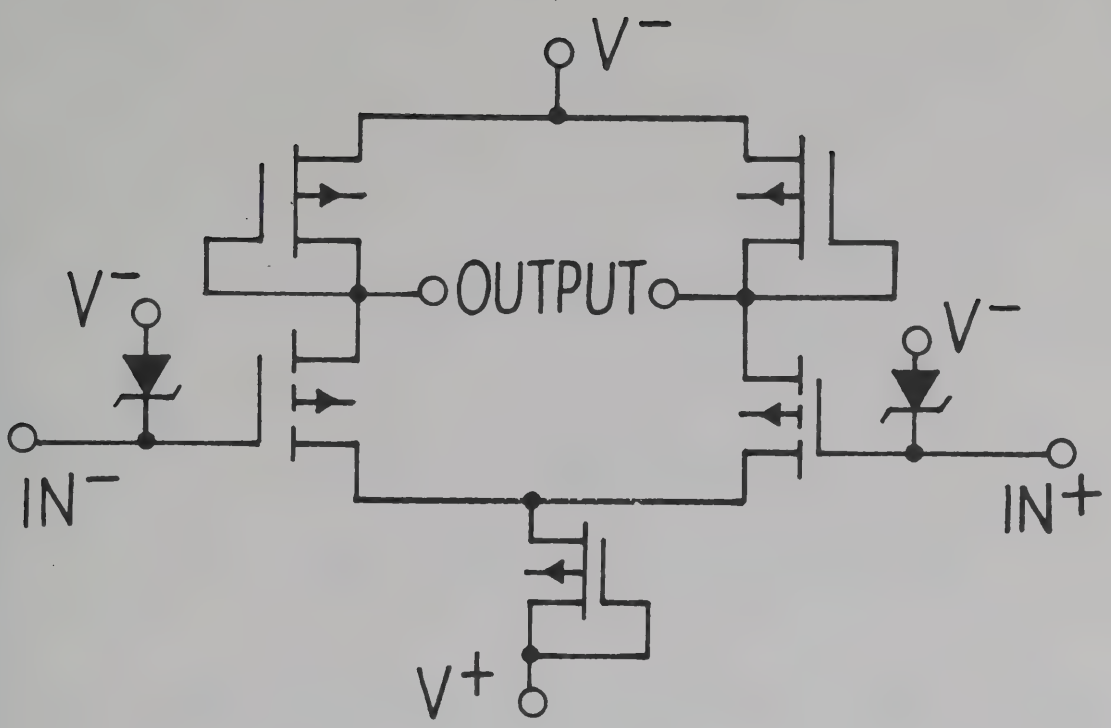



Figure 2.28. Total MOS Amplifier

# Lesson 3

# TRANSLATOR CIRCUITS

*The application of integrated circuits that provides the interface between one logic system of ECL, TTL or MOS to another logic system of a different type, which may be ECL, TTL or MOS, is the subject of discussion.*

# Lesson 3

# TRANSLATOR CIRCUITS

*This lesson discusses interfacing between different digital subsystems with our emphasis on the translation process that converts one set of logic levels to another.*

**Logic Interface** **(Figure 3.1)**

Figure 3.1 illustrates the typical interface problems. One logic system consisting of ECL, TTL, or MOS devices is connected to a second system consisting of ECL, TTL, or MOS devices of a different type.

Voltage level translation can be done with either zener diodes in series with the signal path or by using a common emitter or common collector output that is switched on and off with some intermediate control circuitry.

**Basic Single Polarity Translator** **(Figure 3.2)**

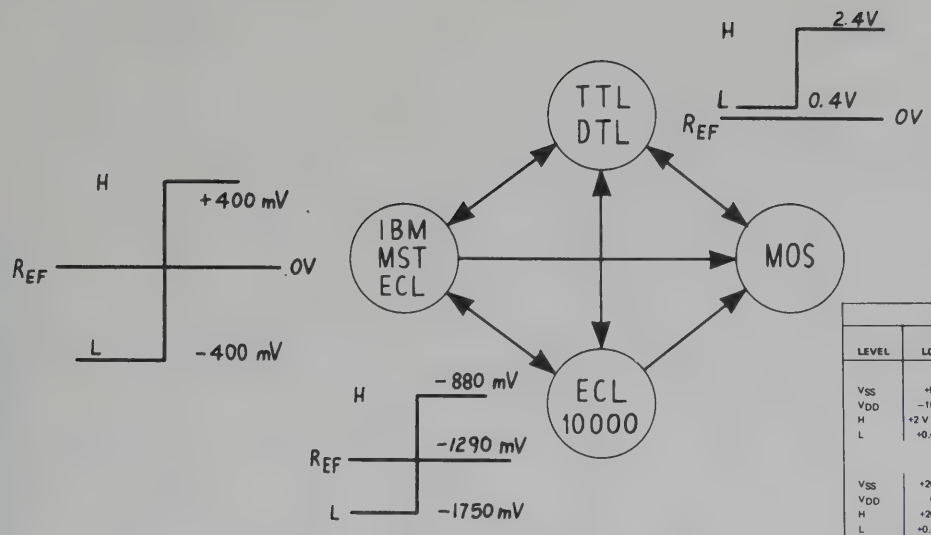
A circuit using a common emitter output to achieve low level to high level translation is shown in Figure 3.2. This simple circuit is a common emitter switch with the pull-up resistor connected to the supply voltage of the high level logic system. It shifts the level of the "1" signal while the level of the "0" signal remains unchanged. The circuit provides an output signal that is of the same polarity as the input signal.

When a change in polarity or a change in both the zero and "1" voltage levels is required, more complex translational circuitry must be used.

**Basic Dual Polarity Translator** **(Figure 3.3)**

The totem-pole output configuration, shown in Figure 3.3, is most commonly used in integrated logic circuits. This type of circuit can act as a translator to any desired positive "1" level and negative "0" by proper choice of $V_{CC+}$ and $V_{CC-}$ supply levels.

This type of circuit is used in many constant voltage mode drivers such as the SN75150 line driver. If there is a need to convert from positive logic to negative logic, translation circuitry of this type could be used to place one logic voltage at ground by making $V_{CC+}$ equal to zero and one logic voltage at the negative $V_{CC-}$. Such an approach would require zener diode translators or a coupling capacitor after the input gate to provide the proper signal levels to the output totem-pole. Another approach is shown in Figure 3.4.




MOS LOGIC LEVEL FAMILIES

| LEVEL | P-CHANNEL LOGIC | P-CHANNEL CLOCK | N-CHANNEL LOGIC | N-CHANNEL CLOCK |
|---|---|---|---|---|
| | | "TTL COMPATIBLE" | | |
| $V_{SS}$ | +5 V | +5 V | 0 V | 0 V |
| $V_{DD}$ | −15 V | −15 V | +5 V | +15 V |
| H | +2 V to 4 V | +4 V | +2 V | +15 V |
| L | +0.4 V | −15 V | +0.4 V | +0.4 V |
| | | HIGH LEVEL | | |
| $V_{SS}$ | +20 V | 0 V | 0 V | −15 V |
| $V_{DD}$ | 0 V | −20 V | +15 V | 0 V |
| H | +20 V | −0.4 V | +15 V | −0.4 V |
| L | +0.4 V | −20 V | +0.4 V | −15 V |

Figure 3.1. Logic Interface

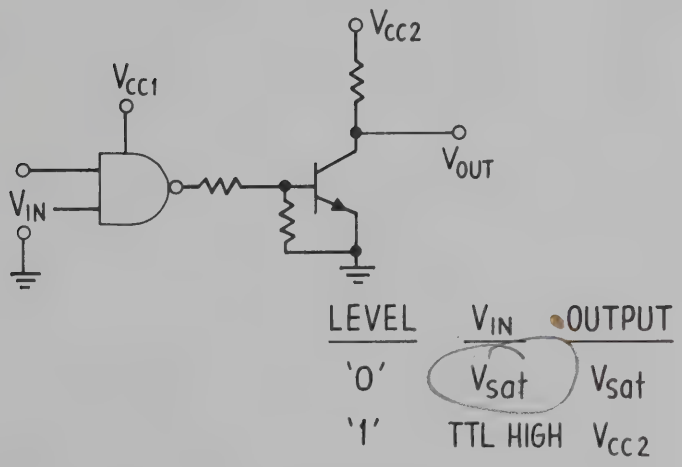



Figure 3.2. Basic Single Polarity Translator

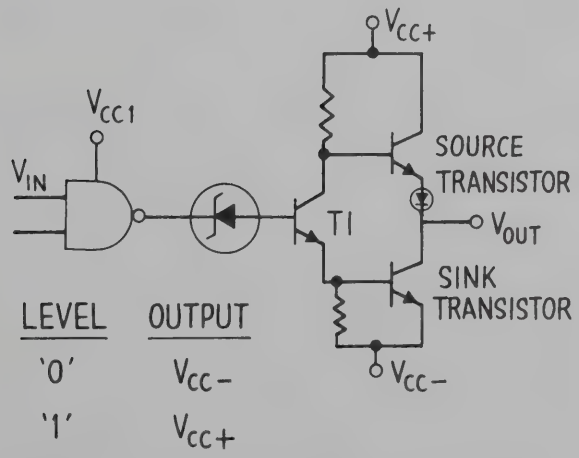



Figure 3.3. Basic Dual Polarity Translator

**Simple Polarity Reversing Voltage Translation** **(Figure 3.4)**

Shown is a P-N-P common emitter output with the pull-up of the P-N-P taken to the negative supply. In this configuration, with the input level low, the gate output would be high and the voltage across the base-emitter junction of the P-N-P would be insufficient to turn the P-N-P on, and the output would be $-V_{CC}$. The logic swing could be changed and the polarity of the logic signals would both be negative.

Next this lesson examines the TTL to MOS translation. This is important because many high density semiconductor memory elements are MOS devices while logic operations are performed by TTL circuits.

**Basic MOS Elements** **(Figure 3.5)**

As shown in Figure 3.5, there are two types of MOS elements, each requiring a special set of logic levels for proper operation. The n-channel FET requires a positive gate voltage to turn the device on. The p-channel FET requires negative gate voltage.

**N-Channel Characteristics** **(Figure 3.6)**

As shown in Figure 3.6, the source-drain path of the device does not become conductive until the gate voltage has exceeded some threshold voltage, $V_T$.

P-channel devices can operate with positive signal if $V_{DD}$ is grounded and $V_{SS}$ is connected to a positive supply voltage.

**Standard TTL Gate Transfer Characteristics** **(Figure 3.7)**

In Figure 3.7, the resulting logic voltage level translation requirements are summarized in terms of the TTL transfer characteristics. If $V_{SS} = 4.5$ volts, then $V_{DD}$ will be ground or 4.5 volts below $V_{SS}$. $V_{GS}$ will be 4.5 minus the TTL output voltage. For proper MOS device operation, the MOS threshold voltage $V_T$ should be between the "0" and "1" output levels of the TTL gate. If the threshold is less than 2.1 volts, both the "0" and "1" TTL output levels would exceed the threshold and be interpreted as a MOS "1" input. If the $V_{GS}$ threshold were greater than 4.1 volts, neither TTL output would be large enough to be a MOS "1" input.

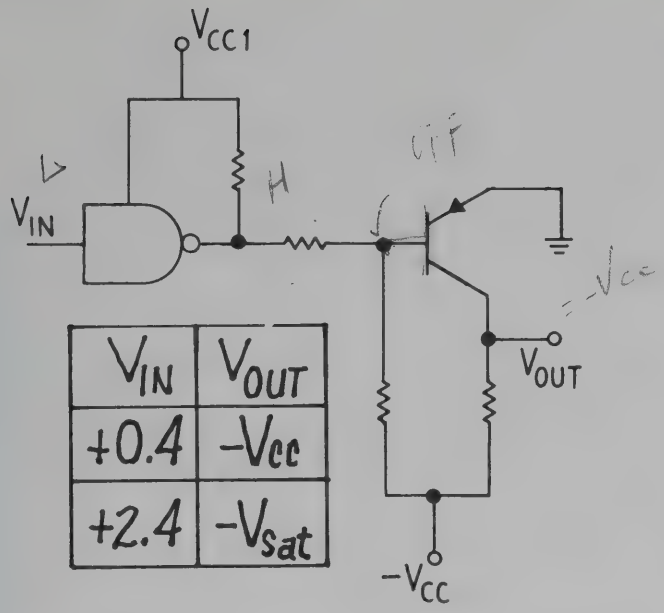



Figure 3.4. Simple Polarity Reversing Voltage Translation

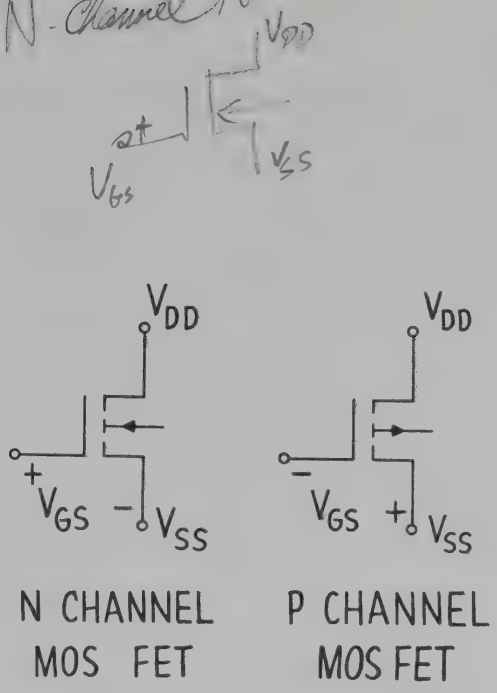



Figure 3.5. Basic MOS Elements

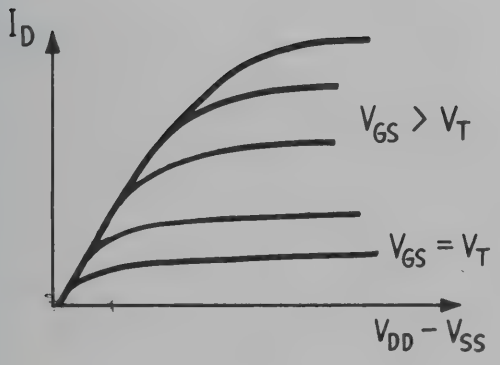



Figure 3.6. N-Channel Characteristics

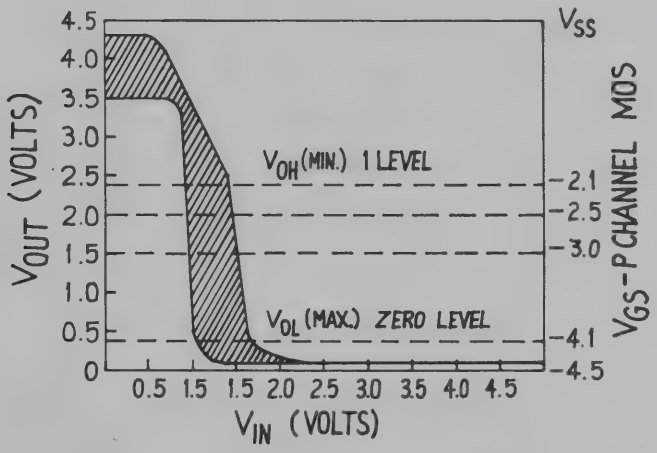



Figure 3.7. Standard TTL Gate Transfer Characteristics

**TTL-MOS Translator Transfer Characteristics** **(Figure 3.8)**

If the MOS device is a high threshold device, the only way to provide a "1" to the device is to increase the output swing of the driver by using one of the special translator techniques discussed earlier. As shown in Figure 3.8, if $V_{SS}$ is equal to the high supply voltage of the translator gate, the MOS input voltage range is increased to 16 volts. Now if the MOS threshold is between 0.5 and 15.6 volts, proper operation of the MOS element is assured.

**Basic TTL to MOS Translator Connection** **(Figure 3.9)**

A basic translator-MOS connection is shown. The pull-up resistor has to be chosen to meet the speed and power requirements of the system as well as to ensure a sufficiently high "1" voltage level for proper MOS operation.

**Typical TTL-MOS Translator Circuits** **(Figure 3.10)**

Some TTL gates with open collector outputs which could be used for this application are listed in Figure 3.10.

Also listed are some drivers and translators that provide a TTL gate, output transistor, pull-up resistor, and separate supply terminals in one package.

**SN75180 TTL-MOS Translator** **(Figure 3.11)**

Shown is the circuit diagram for the SN75180 translator. The "0" level is a negative voltage. The circuit consists of a TTL compatible input gate with a standard TTL supply voltage $V_{CC1}$. This gate switches transistor T2 and thus T3 off and on. With this device, $V_{CC2}$ and $V_{CC3}$ can both be negative, causing negative voltage signals, or $V_{CC3}$ can be positive and $V_{CC2}$ negative, which results in opposite polarity signals for the "0" and "1" outputs. Thus, this circuit could be used to solve almost any negative or dual polarity TTL to MOS translation problem.

The reverse of the problem just discussed is the conversion of MOS type signals from some memory or MOS logic subsystem to signals compatible with the higher speed TTL logic. These require different translator circuit approaches. In many MOS memory elements, output buffer circuits are available to provide direct output to a TTL gate.

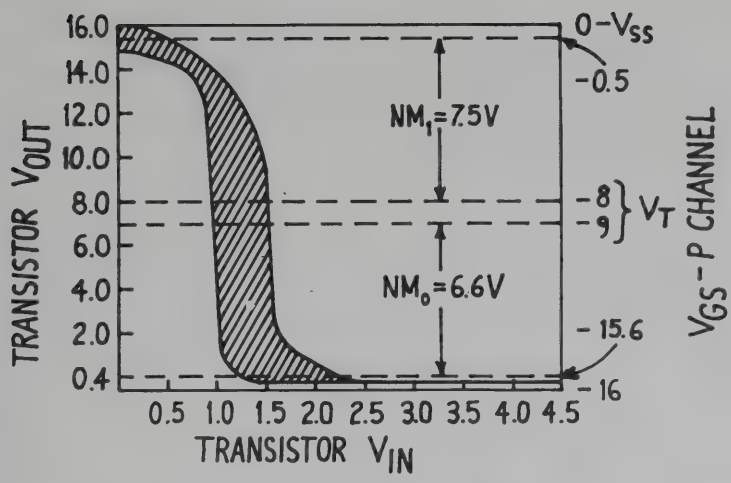



**Figure 3.8. TTL-MOS Translator Transfer Characteristics**

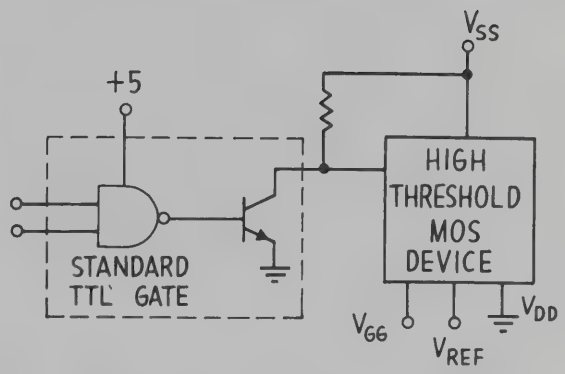



**Figure 3.9. Basic TTL to MOS Translator Connection**

| OPEN COLLECTOR OUTPUT V | | WITH PULL-UP | |
|---|---|---|---|
| DEVICE | OUTPUT V | DEVICE | OUTPUT V |
| SN7450 | 30 | SN75361A | 24 |
| SN7406 | 25 | SN75180 | 30 |
| | | SN75325 | 25 |
| | | SN75365 | 24 |

**Figure 3.10. Typical TTL-MOS Translator Circuits**

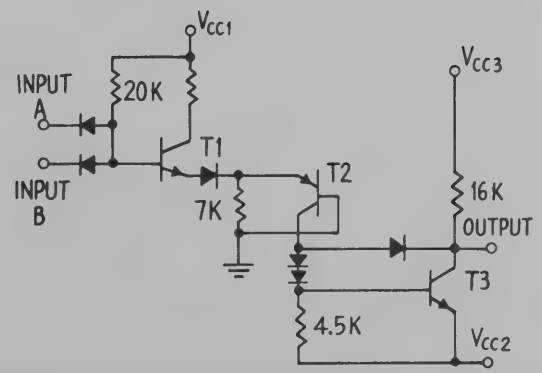



**Figure 3.11. SN75180 TTL-MOS Translator**

**MOS-TTL Translator** **(Figure 3.12)**

For those devices that do not provide such TTL compatible output buffers, the translation can be obtained very simply as shown in Figure 3.12 by using a comparator, sense amplifier, or line receiver that has a TTL compatible output.

**MOS-TTL Translator** **(Figure 3.13)**

Alternatively, a standard MOS-TTL translator circuit, such as the SN75270, can be used to convert an MOS output current of 400 microamps to a TTL compatible signal. MOS circuits that use these types of low current translators include the TMS2600JL, TMS2800JL, TMS1103, and TMS4062.

**MOS-TTL Voltage Translator** **(Figure 3.14)**

For MOS memory circuits which have the conventional high voltage MOS output, a simple voltage divider feeding a standard TTL gate, as shown in Figure 3.14, could be used. For those devices that have a large voltage output the voltage divider usually consists of a 2.7 kΩ resistor feeding a 7.5 kΩ resistor which is tied to −12 volts. The divider output is connected to the input of a standard SN7400 TTL NAND gate.

**TTL Gate Input Characteristics** **(Figure 3.15)**

As Figure 3.15 shows, it is important that these levels be compatible with the SN7400 or other TTL gate input requirements. Obviously, +5.5 volts must not be exceeded or the protective input zener diodes will break down. Similarly, for a "0" voltage of 0.4 volt, the external circuitry must sink 1.6 milliamps. At this current, the "0" level for the divider output circuit would not be −3 volts but nearer to 0 volt.

Another important class of logic translation is that between TTL and emitter coupled logic. These translators are rather specialized circuits as indicated by the ECL2537 converter shown in Figure 3.16.

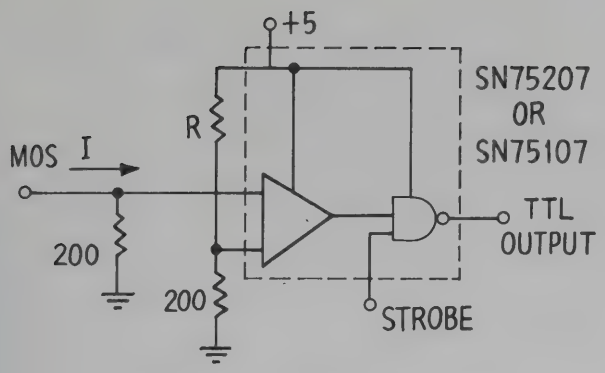



Figure 3.12. MOS-TTL Translator

| I | OUTPUT |
|---|---|
| 10 μA | L |
| 400 μA | H |

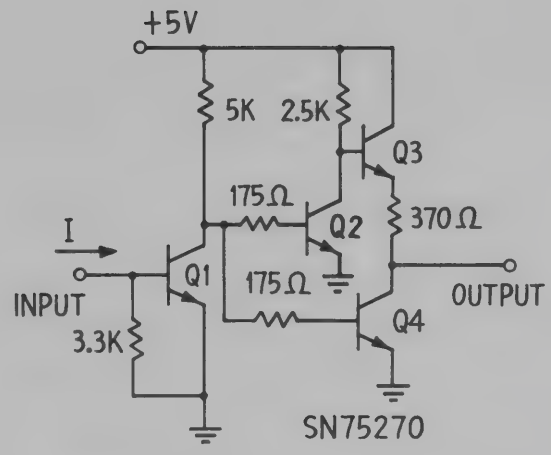



Figure 3.13. MOS-TTL Translator

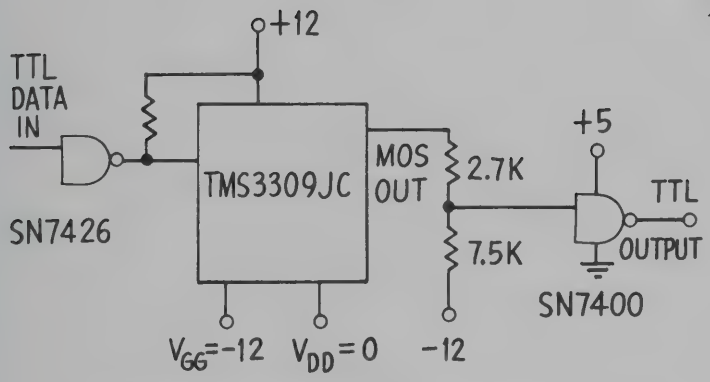



Figure 3.14. MOS-TTL Voltage Translator

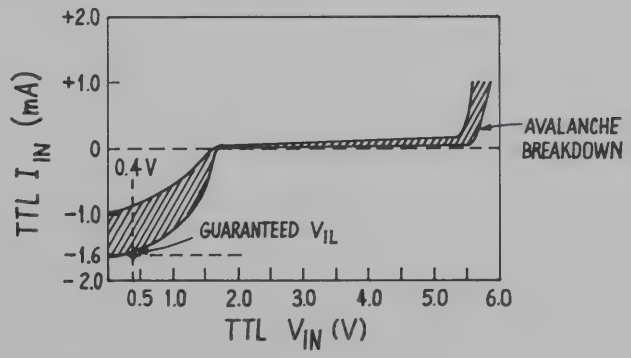



Figure 3.15. TTL Gate Input Characteristics

**The ECL2537–ECL to HLL Converter** **(Figure 3.16)**

The circuit shown in Figure 3.16 is used to convert from IBM MST emitter coupled logic input levels to TTL logic. The logic levels are 400 millivolts for a "1" and –400 millivolts for a "0." The complementary OR-NOR output of the ECL gate is outputted via an emitter follower to yield high level logic voltage levels. A "0" output voltage is from –0.7 to 0.3 volt. Thus the output voltage of this converter circuit can drive directly a TTL gate.

**IC ECL2536–HLL to ECL Converter** **(Figure 3.17)**

The reverse conversion is the high level logic to IBM MST ECL logic. The ECL2536 shown in Figure 3.17 requires 220 microamps of current from both "0" and "1" voltage levels of the high level logic circuit. T3 switches T4 to provide an ECL voltage to the output gate.

**TTL Input to ECL2536 Converter** **(Figure 3.18)**

Shown is an arrangement used to satisfy the input current requirements of the ECL2536. Since the TTL totem-pole sinks current in the low state, the 4.7 kΩ resistor will provide the 200 microamps input to the converter.

The 10000 series of ECL requires –900 millivolt and –1750 millivolt logic levels. Again this requires special translators such as the SN10124 translator shown in Figure 3.19.

**TTL to ECL 10000 Translator** **(Figure 3.19)**

This circuit consists of a DTL input gate, an ECL output gate, and a translator consisting of two forward-biased diodes and two emitter follower amplifiers.

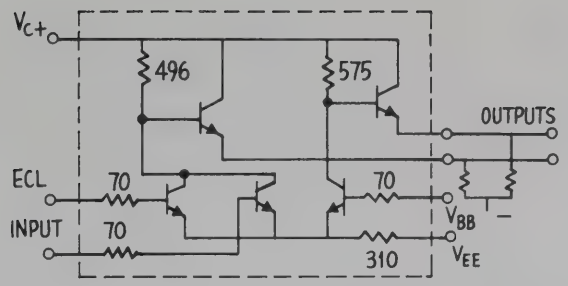



**Figure 3.16. The ECL2537 – ECL to HLL Converter**

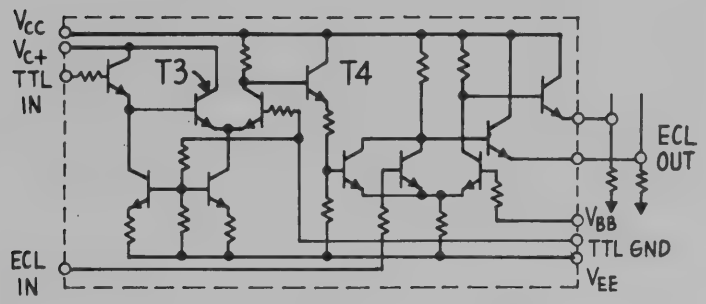



**Figure 3.17. IC ECL2536 – HLL to ECL Converter**

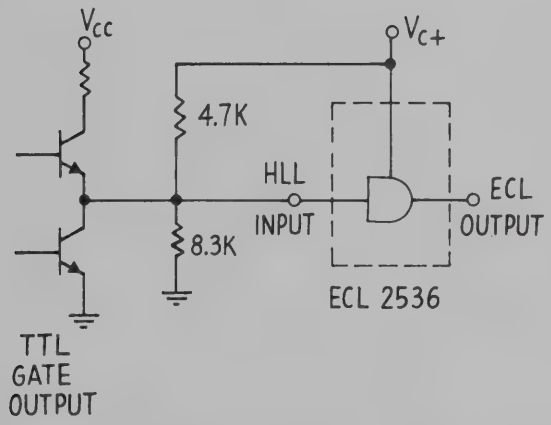



**Figure 3.18. TTL Input to ECL 2536 Converter**

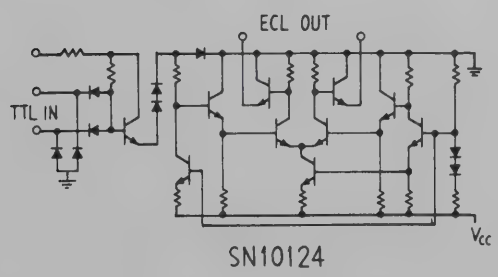



**Figure 3.19. TTL to ECL 10000 Translator**

**ECL 10000 to TTL Translator** **(Figure 3.20)**

As shown in Figure 3.20, for translation from ECL 10000 to TTL, the ECL SN10125 ranslator can be used. Here the ECL input gate switches the constant current source to turn n the source or sink output in the standard TTL totem-pole output configuration.

In order to convert from the 10000 type of ECL gate to the IBM MST ECL, the N10184 and SN10185 translators are available between the +400 millivolt, −400 millivolt vels of the IBM MST systems to the −900 millivolt, −1750 millivolt 10000 series logic vels. Circuit input and output impedance and current requirements are met along with the gic level requirements so that the exact device input and output properties do not have to e determined separately.

One final important area is the interfacing between ECL and MOS devices. This class of terface problems is complicated by two different types of ECL circuits as well as two fferent types of MOS devices. There are not any interface circuits that will convert MOS gic signals directly to ECL logic signals. Some voltage divider technique must be used to put to the ECL2536.

The SN75368 provides the required interfacing from ECL to MOS for both 10000 ies and IBM MST logic levels. The basic parts of these circuits are shown in Figure 3.21.

**put/Output Configuration for ECL to MOS Translator** **(Figure 3.21)**

These provide an ECL gate which can be connected to either the IBM MST supply els or the 10000 series supply levels to provide input signal compatibility with these rices.

**MMARY**

Emphasis in this session has been on the translator circuits, though several drivers that be used as translators have been discussed.

All basic types of presently available integrated circuit translators have been covered can interface among TTL systems, MOS systems, and ECL systems.

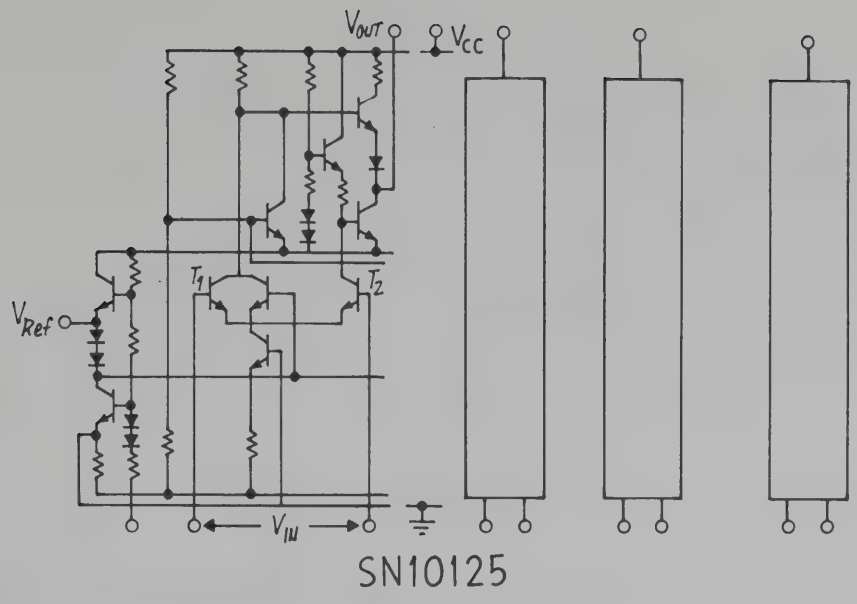



**Figure 3.20. ECL 10000 to TTL Translator**

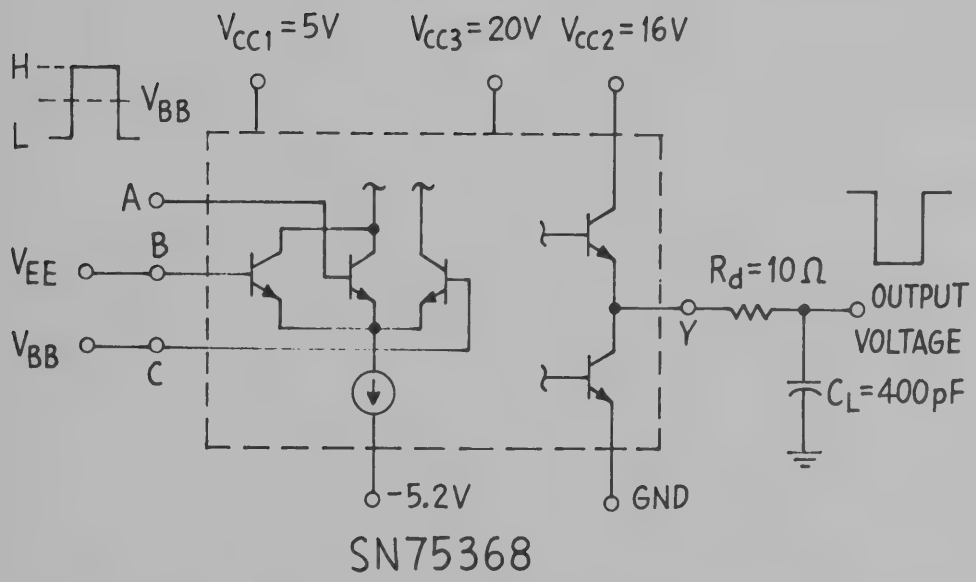



**Figure 3.21. Input/Output Configuration for ECL to MOS Translator**

# Lesson 4

# GENERAL PURPOSE DRIVER CIRCUITS

*The applications of interface integrated circuits as devices for high capacitive loads, inductive loads, electromechanical elements such as solenoids, relays, printers – including the thermal printer – and VLED displays are demonstrated by specific examples.*

# Lesson 4

# GENERAL PURPOSE DRIVER CIRCUITS

*One of the more important devices in the class of interface circuits is the integrated circuit driver. This type of element is used to connect system signals to the system output elements or memory storage elements to communicate between low level system signals and external elements requiring high driver power.*

**Driver Applications** **(Figure 4.1)**

Applications of these devices considered in this session include the areas shown here. Driving a large number of gates requires a driver with a high fan-out capability. The MOS memory driver is an important group of circuits to utilize the economical high speed semiconductor MOS memories that are presently available. Such a device generally requires a translator as well as a driver for proper memory operation. The requirement to input data into a core memory is an important area requiring relatively high drive currents. The display drivers include VLED drivers which in some cases require a matrixing capability of the same type used in core memory drivers.

**Low Level to High Level Voltage Translation** **(Figure 4.2)**

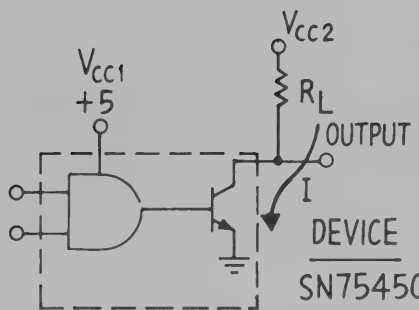
The basic voltage translation is illustrated here where the open collector transistor output can be returned to a $V_{CC2}$ that is higher than the 5-volt output of the TTL gate. Then, with the input gate high, the output transistor is saturated so that the low output level is $V_{sat}$. With the input gate low, the output transistor is off with the output high level being $V_{CC2}$ minus $R_L$ times the leakage of the output transistor.

**MOS System Input Model** **(Figure 4.3)**

TTL-MOS drivers and the basic requirements on these circuits in inputting data into lines or capacitive loads can be summarized by considering the equivalent circuit shown here. Each MOS element input circuit consists of a gate capacitance in parallel with a gate resistance. Since $R_g$ is generally in the gigaohm range or more, the $R_{in}$ is sufficiently large for a practical number, N, of parallel MOS elements that it can be considered an open circuit.

- HIGH FANOUT LOGIC DRIVERS
- MOS MEMORY DRIVERS
- CORE MEMORY DRIVERS
- DISPLAY DEVICE DRIVERS
  - VLED'S AND INCANDESCENT DEVICES
  - GAS DISCHARGE AND ELECTRO LUMINESCENT DEVICES
- POWER ELEMENT DRIVERS
  - ELECTROMECHANICAL ELEMENTS
  - THERMAL ELEMENTS

**Figure 4.1. Driver Applications**




| DEVICE | $V_{CC_2}$ (VOLTS) | $I_{MAX}$ (mA) |
|---|---|---|
| SN75450 | 30 | 300 |
| SN75325 | 24 | 600 |
| SN7406 | 25 | 40 |
| SN75326 | 24 | 600 |

**Figure 4.2. Low level to High Level Voltage Translation**

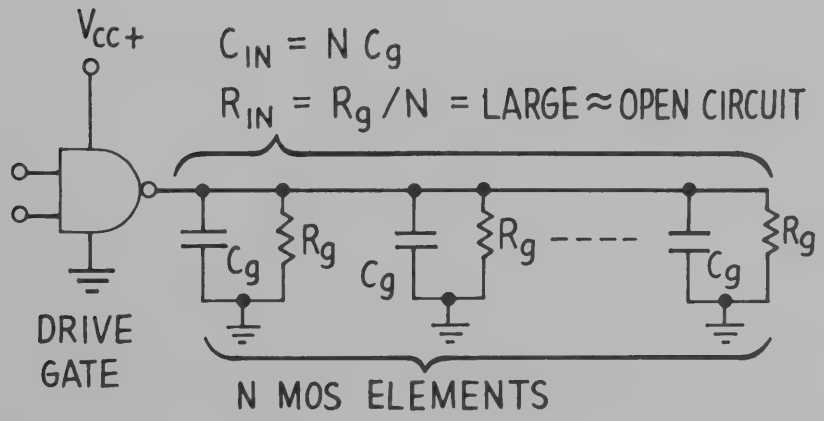



**Figure 4.3. MOS System Input Model**

**MOS Constant Voltage Driver** **(Figure 4.4)**

The gate capacitance must be charged to a "1" level or discharged to a "0" level by the drive gate output in order to change the MOS state. This can impose severe current requirements on the drive as can be computed from the overall equivalent circuit shown here for a constant voltage driver. The corresponding change in voltage depends exponentially on time with the rise and fall times typically 2.2 times the $R_dC$ time constant. The current is C times the derivative of the voltage. $\Delta V$ is the difference between the "0" and "1" voltage levels on the input to the MOS element.

**MOS Driver Current for Constant Voltage Mode Driver** **(Figure 4.5)**

These requirements are plotted here. The driver must either drive or sink $\Delta V$ divided by $R_d$ or 2.2 times C times $\Delta V$ divided by rise time. As C increases, or as the required rise time decreases, the driver current and power can increase beyond reasonable limits. This may require several drivers in parallel or external power transistors with heatsinks.

**MOS Constant Current Driver** **(Figure 4.6)**

If the driver is a constant current driver in both the source and sink modes, the driver mode must be changed to a constant current type of circuits as shown here. With $R_d$ assumed large, the voltage changes linearly with time. A high C or short rise time requires higher driver currents.

**Driver Current and Power Requirements** **(Figure 4.7)**

The driver power can be obtained from the expression $I_d$ by multiplying by $\Delta V$ to yield these expressions. In both types of drivers, the power and current requirements increase with increasing $\Delta V$, increasing capacitance, and increasing frequency of operation. Some drivers act as a combination constant voltage and constant current mode driver since they have current limiting features in both the source and sink modes. The pull-up resistor can severely limit the obtainable rise time and frequency for a given load capacitance.

As an example application of such capacitive loads, consider the driving of a 900 pF load at a data rate of 2 MHz. If 40 nanoseconds is allowed for a state change, such a load would require a peak current of over 200 milliamps for a constant current driver and over 700 milliamps for a constant voltage driver. Either driver would require a power of 200 milliwatts for an operating frequency of 2 megahertz.

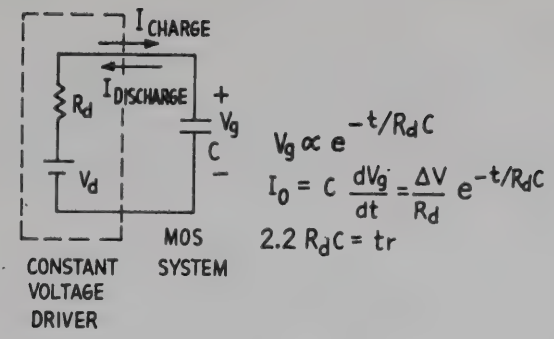



**Figure 4.4. MOS Constant Voltage Driver**

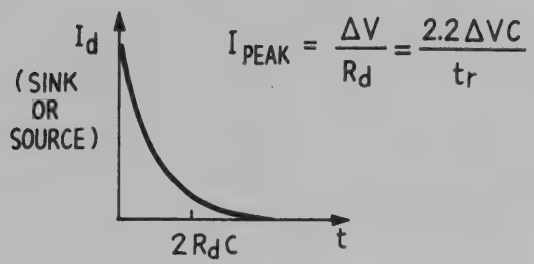



**Figure 4.5. MOS Driver Current for Constant Voltage Mode Driver**

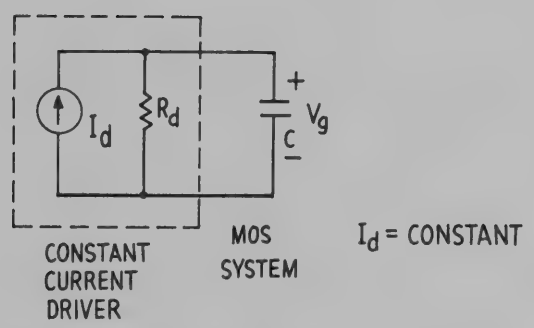



**Figure 4.6. MOS Constant Current Driver**

| | CONSTANT CURRENT | CONSTANT VOLTAGE | GENERAL |
|---|---|---|---|
| $I_{PEAK}$ | $.8\frac{C\Delta V}{t_r}$ | $2.2\frac{C}{t_r}\Delta V$ | $\approx fC\Delta V$ |
| POWER | $\frac{.8C\Delta V^2}{t_r}$ | $2.2\frac{C}{t_r}\Delta V^2$ | $\approx fC\Delta V^2$ |

**Figure 4.7. Driver Current and Power Requirements**

**SN75361 Driver Characteristics** **(Figure 4.8)**

If an SN75361 driver which has a current output capability of 100 milliamps and 400 milliwatts/driver is to be used in this application, two of these driver elements would be required in parallel for this load. As shown, this driver can safely drive only up to 450 pF at a 2 megahertz rate with a 40 nanosecond propagation delay.

The SN75326 driver offers 600 milliamps current and a 800 milliwatt power output with a 24-volt voltage mode driver thus enabling one such driver to drive the full 900 pF load. The SN75450 dual peripheral driver has an output that could drive the 450 pF load.

**Sink-Source Drive-Biased Core Line** **(Figure 4.9)**

Another common problem is the driving of inductive loads such as driving magnetic memory elements, printer head solenoids, relay, and so forth. For those devices that require both directions of a possible high current and some method of selecting which device is to be driven, one possible connection is utilizing a source-sink pair or a totem-pole driver as shown. With the source on and the sink off, this circuit could drive current through the device in one direction; and with the sink on and the source off, the driver would provide the current in the opposite direction. This network does require a +5 volt bias supply for the device drive lines.

**Inductive Load Driver** **(Figure 4.10)**

This could be avoided by using the same circuit with the device drive line grounded and the sink transistor emitter connected to a negative supply. An example of such a connection is shown with an SN75450 peripheral driver. The diodes ensure proper direction of current flow and protection from voltage spikes. The sink and source will be enabled separately and in a complementary fashion so that the case of having both sink and source transistors on simultaneously can be avoided.

**Source-Sink Drive-Unbiased Load Line** **(Figure 4.11)**

The requirement of negative supplies and a biased load line can be avoided by using the configuration shown. By selecting source 1 and sink 2, positive current will flow through the load from left to right, and by selecting source 2 and sink 1, the current will flow from right to left through the load. Selecting neither leaves the load line open circuited at both ends.

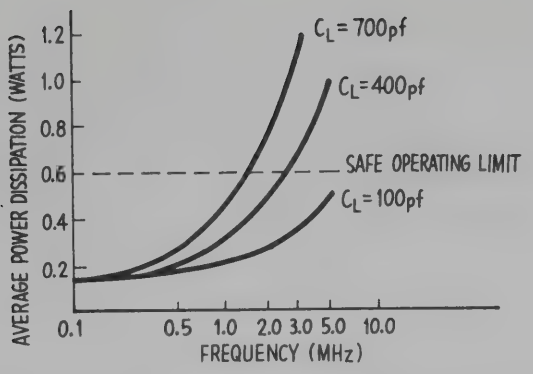



**Figure 4.8. SN75361 Driver Characteristics**

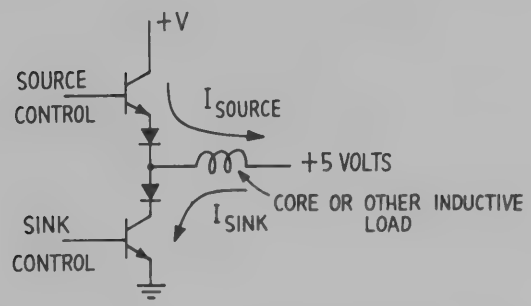



**Figure 4.9. Sink-Source Drive-Biased Core Line**

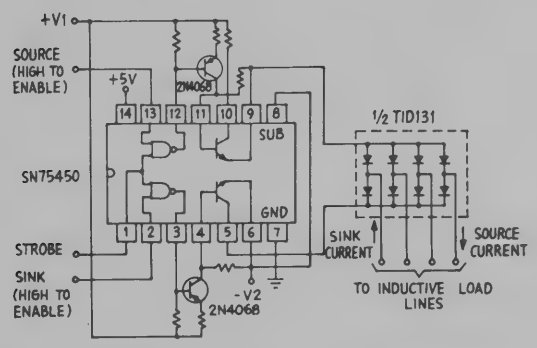



**Figure 4.10. Inductive Load Driver**

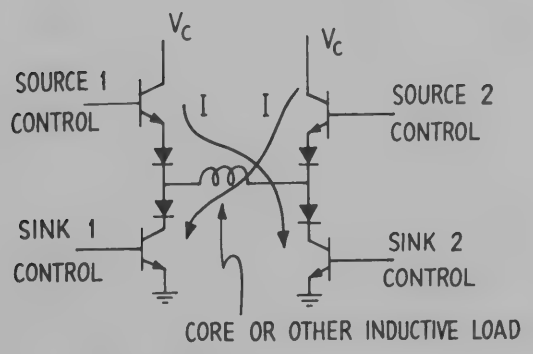



**Figure 4.11. Source-Sink Drive-Unbiased Load Line**

**SN75325 as Matrix Load Driver** **(Figure 4.12)**

This configuration can be illustrated by using the 600 milliamp SN75325 core driver. The input gates are selected by a standard TTL gate from a TTL address decoder, such as the SN74154. Two gates are selected as sources or two are selected as sinks by the mode control. Another similar circuit would then select the other sink or source to be activated.

**Relay Driver Application** **(Figure 4.13)**

In many inductive load applications, there are no dual polarity current requirements. One such application is the driving of a relay coil. The use of the relay allows the control of a very high power output device almost directly from low level logic system.

**SN75270 as MOS Sense Amp and Thermal Print Head Predriver** **(Figure 4.14)**

Some applications, such as driving line printer heads or thermal print heads, need more current capability than can be provided by an integrated circuit driver. External power transistors can be driven by one of the integrated circuit drivers. In this example, the SN75270 is used to interface between a MOS calculator chip and the power transistor that directly drives the thermal print head devices.

**Seven-Segment Numerical Display** **(Figure 4.15)**

The driver matrixing techniques can be used to advantage in many applications for driving optical display devices, such as VLEDs. These devices are composed of light emitting diodes that require from 1 to 10 milliamps per diode. Each diode geometry is of the form of a straight line segment with seven segments required to make any numeral from 0 to 9.

**MOS-VLED Interfacing** **(Figure 4.16)**

A given segment in a given digit can be selected by using matrixing techniques similar to the ones used on inductive loads. The digit driver is connected to all segments of a given digit. By selecting a given set of segment drivers and a given digit driver, a specific numeral will be displayed in that digit position on the display.

The selection control is provided by the MOS TMS0100 calculator chip with the SN75492 drivers as a sink driver and the SN75491 acting as a source driver. These drivers also simultaneously solve the MOS interface problem. Since in cases such as this, only one digit is to be displayed, it is advisable to time multiplex the entire set of digits at such a rate that the resulting dynamic display seems to be continuous to the viewer's eyes. Such a dynamic display lowers the display power requirements considerably without sacrificing visual display quality.

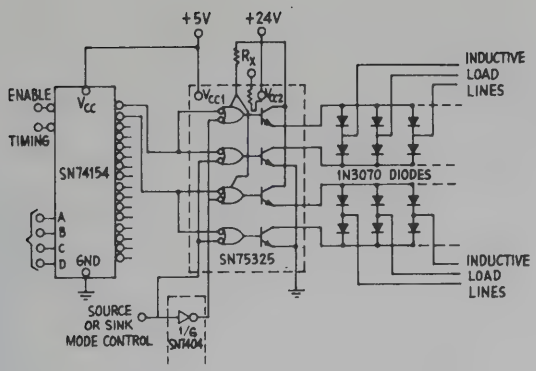



Figure 4.12. SN75325 as Matrix Load Driver

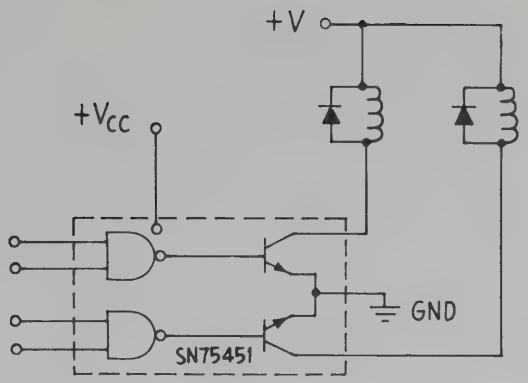



Figure 4.13. Relay Driver Application

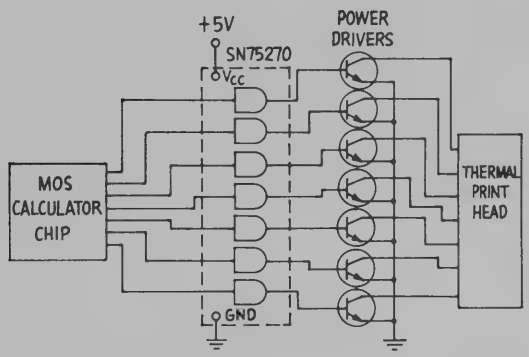



Figure 4.14. SN75270 as MOS Sense Amp and Thermal Print Head Predriver

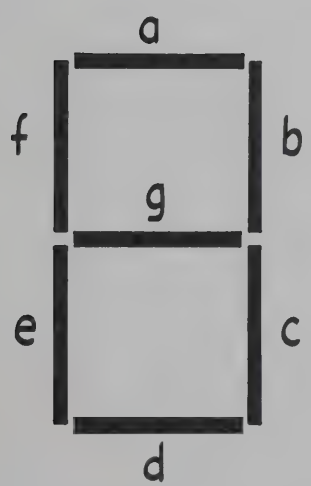



Figure 4.15. Seven-Segment Numerical Display

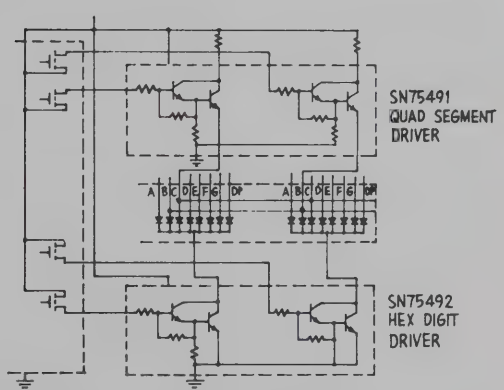



Figure 4.16. MOS-VLED Interfacing

**Direct Seven-Segment Display Driver** **(Figure 4.17)**

If interfacing out of a MOS shift register in a nonbattery power system, a continuous display may be preferred. In this case, it is advisable to provide a BCD to seven-segment decoder which can directly drive each seven-segment device. The basic configuration in using these direct display drivers is shown here. In this case, the output of a decade counter or BCD arithmetic unit is placed in the SN7475 buffer BCD storage register, which in turn is connected to the BCD to seven segment decoder. The decoder outputs drive the proper segment lamp or diode of the seven-segment display device to display the number stored in the buffer register.

**Driving High Voltage Display Devices** **(Figure 4.18)**

In cases where either very high voltage output or high power output with fast switching times is desired, solid state power elements such as SCRs and TRIACs are used. An example of using an SCR to control the high voltage is shown here. The SN7448 or SN7449 BCD to seven-segment decoder driver is used to control the SCR. If the output of a segment driver is low or $V_{sat}$, the SCR is off and there is no voltage applied to the display segment. When the driver output voltage goes toward $V_{CC}$, the SCR turns on, and the full high voltage supply voltage appears across the display segment, turning it on.

**TTL Compatible TRIAC Driver** **(Figure 4.19)**

Integrated circuit drivers can control TRIACs which can, in turn, handle high voltage or high power loads. An example configuration is shown here. Controlling the duty cycle into the SN75450 gate driver thereby controls the duty cycle of the high power or high voltage applied to the load.

**SUMMARY**

The integrated circuit drivers offer almost unlimited opportunities for outputting the information contained in digital logic and arithmetic systems to display, transmission, memory, or power control devices.

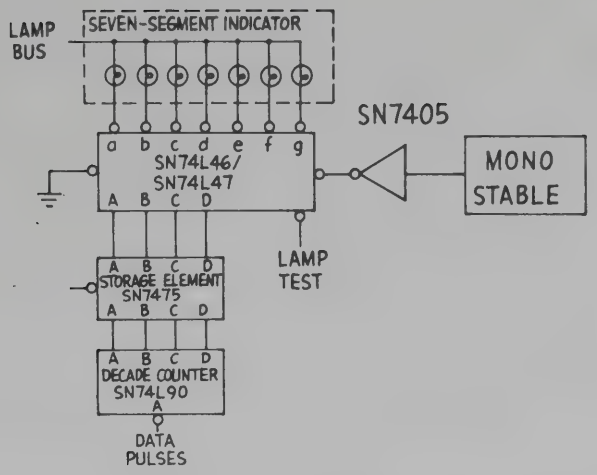



Figure 4.17. Direct Seven-Segment Display Driver

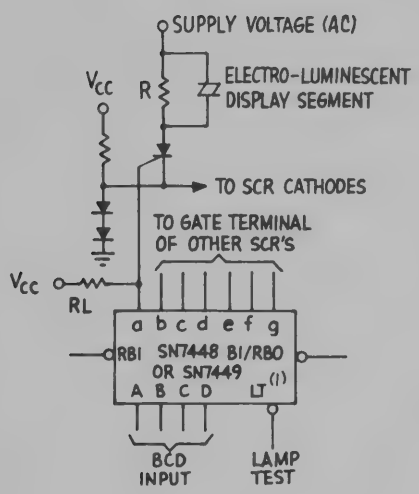



Figure 4.18. Driving High Voltage Display Devices

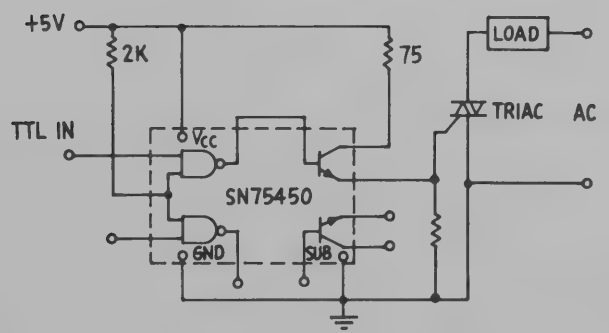



Figure 4.19. TTL Compatible TRIAC Driver

# Lesson 5

# CORE MEMORY DRIVER APPLICATIONS

*Magnetic core drivers must provide high current with good high frequency performance. Special integrated circuits have been designed for this interface. This session discusses these applications.*

# Lesson 5

# CORE MEMORY DRIVER APPLICATIONS

*Our subject is core memory driver applications. Such drivers are specifically designed to drive inductive loads. As a result, they provide high current with good high frequency performance, as well as good breakdown voltage characteristics to withstand the reverse voltage inherent in inductive circuits. In addition, these monolithic circuits are specifically organized or packaged to fit the electrical and packaging organization of the core memory systems.*

*To readily understand the use of the integrated circuit drivers, one must first understand the basic core characteristics, some of the definitions of the currents required, and some of the basic core system organizations.*

**Basic Storage Core** **(Figure 5.1)**

The basic storage element is a lithium ferrite core shown here. Two wires pass through it and connect as shown. One is for sensing an output voltage and the other for driving a current $I_H$.

**B-H Curve** **(Figure 5.2)**

This is a so-called B-H curve, or rectangular hysteresis loop. Note that the magnetizing force, H, is generated by and is proportional to I. The one state and zero state designations are arbitrary. However, if no current flows in the drive circuit, the core is left with residual flux and will be either at the one or zero state depending on the direction of the current that set it initially.

Start with the core at the zero state. A current of positive $I_H/2$, called a partial write current, $I_{pw}$, will not materially change the magnetic flux of the core; however, an abrupt reversal of flux direction results when the magnetizing force exceeds a critical value in the right direction.

With a current of $+I_H$, called a full write current, $I_W$, the core flux switches and then falls back to the one state. With the core in the one state, a current of $-I_H/2$ called a partial read current, $I_{PR}$, does not change the core, but a full read current of $I_R$ switches the core and leaves it in the zero state.

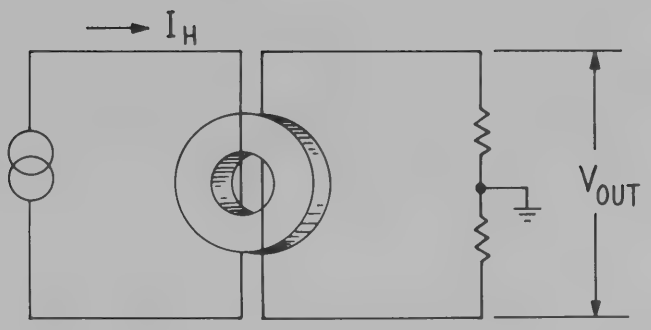



Figure 5.1. Basic Storage Core

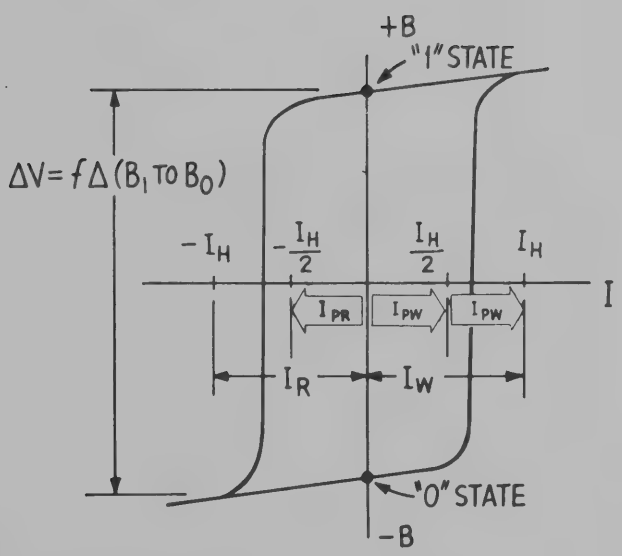



Figure 5.2. B-H Curve

The critical magnetizing forces for saturating the core can be generated by the addition of force in the same direction from a number of wires passing through the core. Or conversely, critical magnetizing forces can be prevented from accumulating by subtracting forces with opposing currents in multiple wires passing through the core. This logic has produced either a small change in flux or a large, abrupt change in flux. This flux change generates the sense voltage.

**Sense Voltage** **(Figure 5.3)**

Here is the sense voltage. The output voltage is small when only a partial read current is applied. It is, however, large when initially in a one state and the core is switched to the zero state, but still small if the core was initially in the zero state.

**3D-4W System** **(Figure 5.4)**

The core of this 3D-4Wire system has an X wire, a Y wire, a sense wire and a Z wire or inhibit line. The particular bit stored in read out from the desired location by having a coincidence of $I_{PR}$ currents in the X and Y wires.

**Coincident Current** **(Figure 5.5)**

Both the $I_X$ and $I_Y$ are $I_{PR}$ and a critical magnetic force switches the core because it was in the one state and a large sense voltage is detected to read the one stored. The one was written into the core at the desired location by having a coincidence of $I_{PW}$ currents in X and Y lines. To prevent the one from being written or stored, a counter or opposing current of $I_{PR}$ is passed through the inhibit wire at the same time that $I_{PW}$ appears on the X and Y wires. This leaves the core in the zero state. It always is in the zero state after a read instruction.

If there is no coincidence of either the partial read or partial write currents in the X and Y wires through the core, then the core is not selected. This is why the 3D core memory is called a coincident current memory.

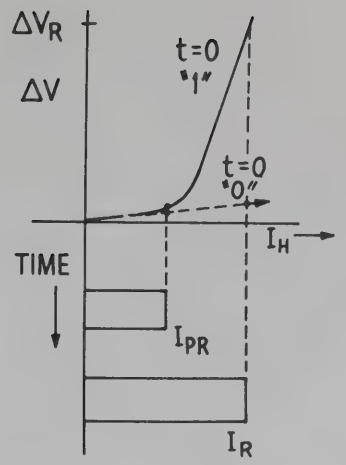



Figure 5.3. Sense Voltage

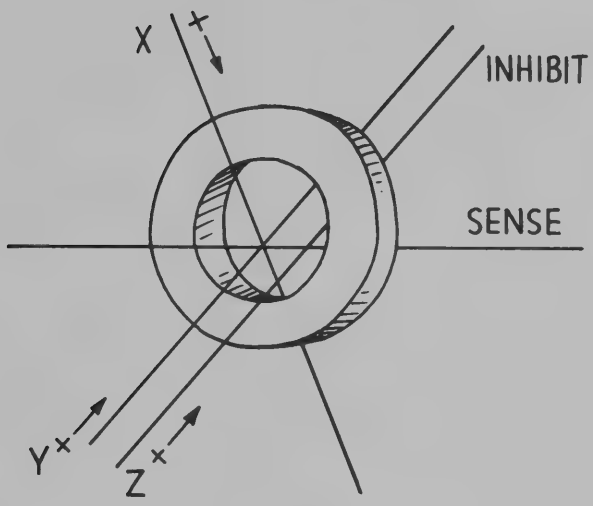



Figure 5.4. 3D-4W System

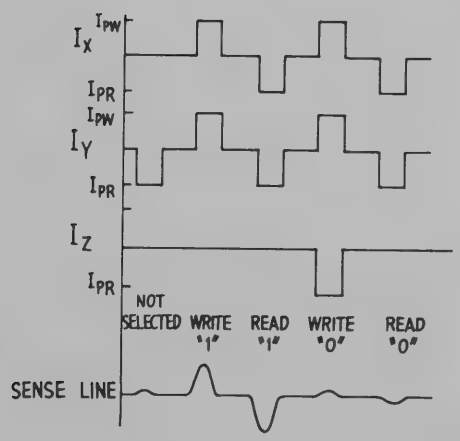



Figure 5.5. Coincident Current

**3D Core Planes** **(Figure 5.6)**

Here are three core planes of the 3D core system. The number of cores in the plane is the number of words. The number of planes is the number of bits. Like core positions are selected by the coincidence of the current in the X and Y wires. The sense winding weaves through every core on the plane. The information on it in a given read time is the bit position information of the word selected. The inhibit winding is common to all cores in the plane. But recall that only a current in one direction of $I_{PR}$ flows in this wire; not $I_{PR}$ and $I_{PW}$.

By using the sense line to perform the inhibit function, the 3D-4W systems have been changed to 3D-3W systems. Thus, a wire is omitted through each core, and peripheral circuits are simplified.

**3D Core System Expansion** **(Figure 5.7)**

This shows a further expansion of the 3D core system. The sense amplifiers detect the information. The inhibit drivers are included with the sense amplifiers if the system is 3D-4W. The inhibit drivers are as shown in dotted lines if the system is a 4-wire system. The X drivers have address decoding, read/write, and timing control associated with them; likewise for Y drivers. Note that both the X and Y drivers must have drivers for supplying current as well as drivers to sink the current. This is because the coincident currents, $I_{PR}$ and $I_{PW}$, must be in opposite directions.

Recall that the core always goes to the selected initial state – in our discussion the zero state – after being read. Therefore, the read function must be followed by a write function because the reading function is destructive.

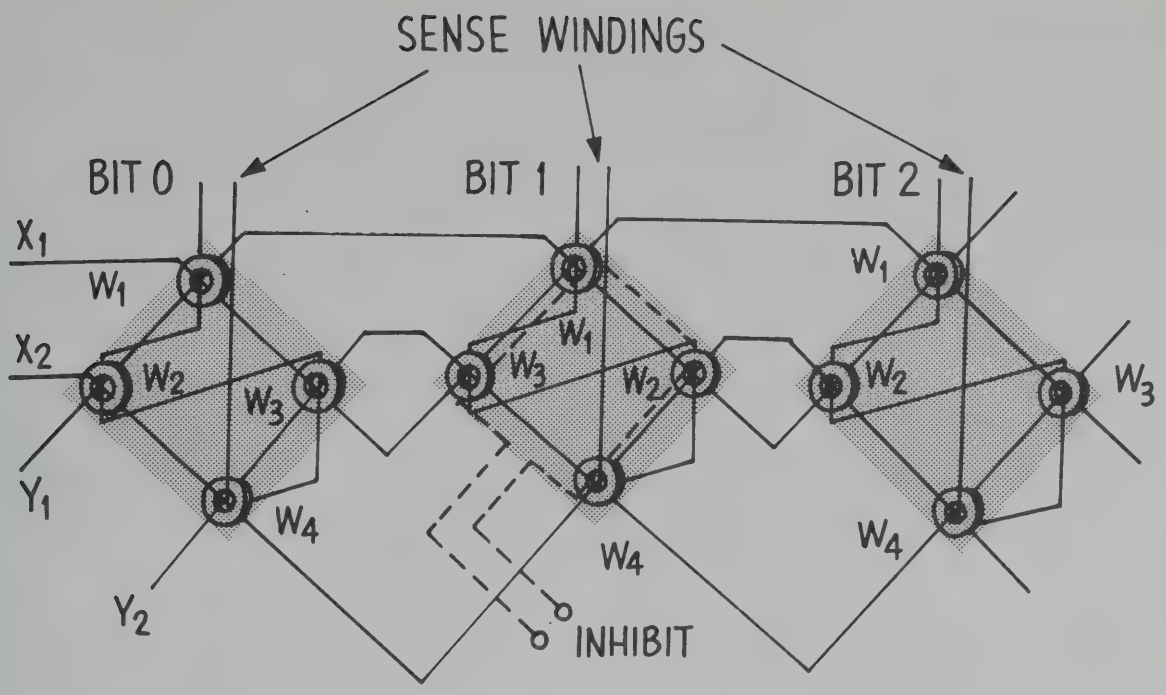



Figure 5.6. 3D Core Planes

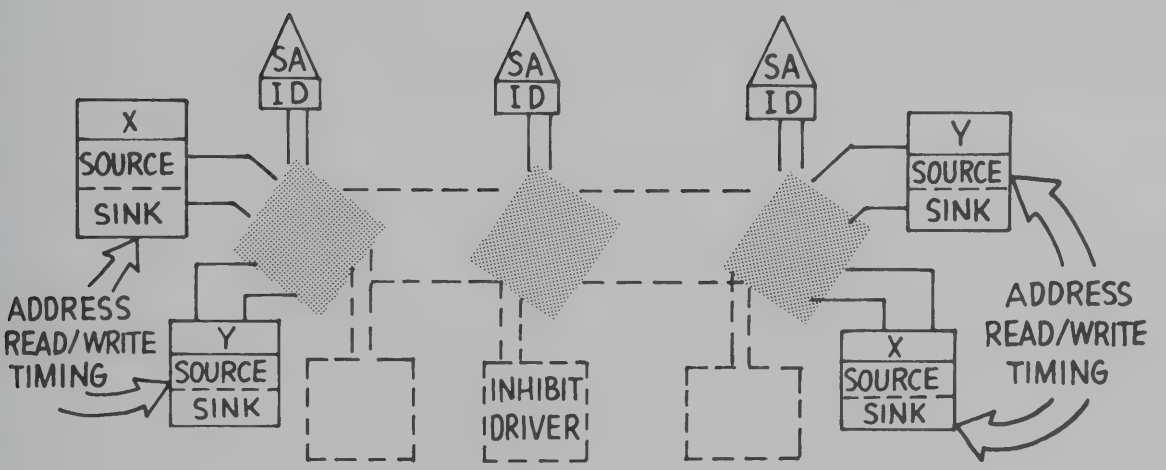



Figure 5.7. 3D Core System Expansion

**2D Core** **(Figure 5.8)**

This figure shows the way the cores are arranged in a one-core per bit 2D system. There are only two wires through the core for selection and writing information. In addition a sense wire is included through the same cores as the bit lines. However, there are some mass memories that sense on the bit lines because they are striving for low cost, and maximum speed performance is no problem. The word line, identified with a W, links the number of cores, that is, bits, in the word and a driver only drives current in one word of the array. The bit line links all cores that represent the same bit position in the word.

**2D Read and Write Currents** **(Figure 5.9)**

During read, a current equal to $I_R$ or greater is supplied to the selected word line and every bit in the word is read. Significant overdrive can be used to achieve extremely fast switching times. Circuit and power dissipation are then the limiting items.

During write, coincident partial currents, $I_{PW}$, are required in the word and bit lines if the data to be stored is a one. Omitting the $I_{PW}$ current in the bit line performs the inhibit function and a zero results. Therefore, current must flow in both directions in the word line but only in one direction through the bit line.

**2D Core System** **(Figure 5.10)**

The core array contains W words times B bits. Source and sink drivers are required on the word lines. Read/Write control and timing, as well as address decoding, are required. The same kind of drivers and sense amplifiers can be used in the bit direction as for the 3D systems. For reference, the 2D system is also called a linear select or word organized system.

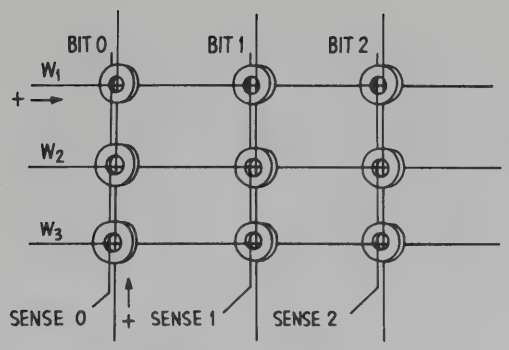



Figure 5.8. 2D Core

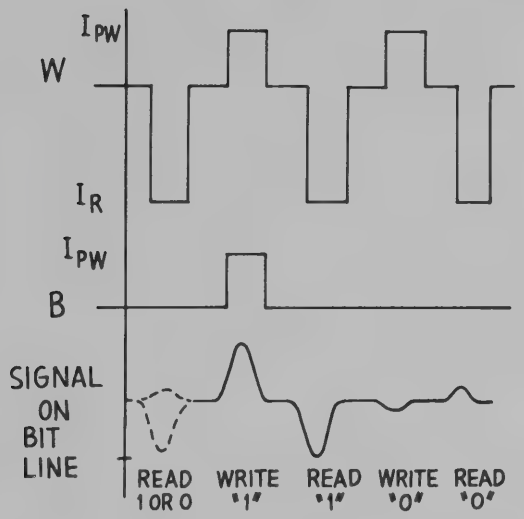



Figure 5.9. 2D Read and Write Currents

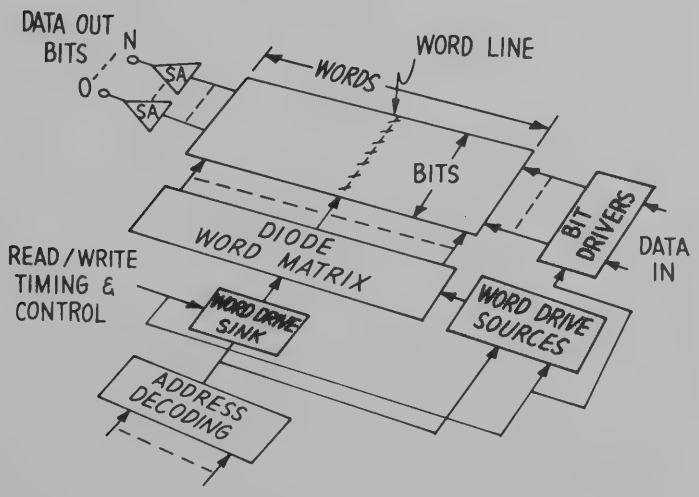



Figure 5.10. 2D Core System

**2-1/2D Core** **(Figure 5.11)**

Here is the electrical and physical assembly of the cores of the 2-1/2D system. The 2-1/2D system receives its designation from the fact that it is a hybrid system having features of both the 3D and 2D systems.

**2-1/2D Read and Write Currents** **(Figure 5.12)**

The X and Y lines now need coincident partial $I_{PR}$ currents to read and partial $I_{PW}$ currents to write a one. This is the same as the 3D system. Writing a zero is accomplished by omitting the $I_{PW}$ current on the respective Y line for that bit.

Look at Figure 5.11 again. The X lines are in somewhat the same arrangement as for the 3D system but the Y lines are separated for each bit plane with a driver. $Y_0'$, $Y_1'$ and $Y_2'$ are activated at the same time, thus providing the coincident current for all bits that are to be selected.

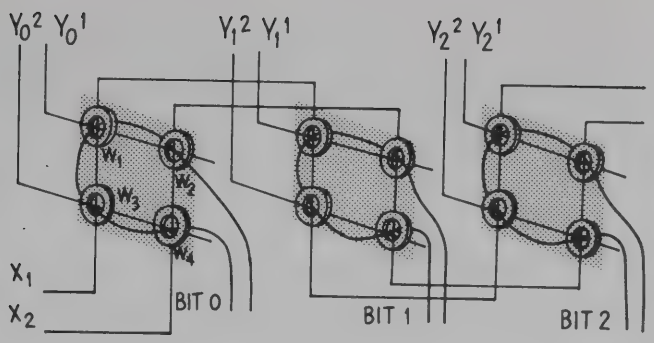



**Figure 5.11. 2-1/2 D Core**

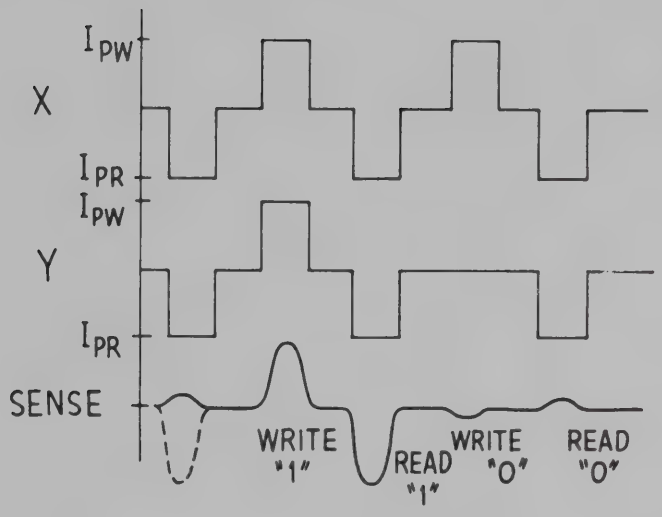



**Figure 5.12. 2-1/2D Read and Write Currents**

**2-1/2D Core System** **(Figure 5.13)**

This figure shows the type and location of the drivers for the 2-1/2D system. The X and Y drivers are bidirectional and need both a source and a sink. The same amplifiers are shown but no inhibit drivers are required.

**Bidirectional Driver** **(Figure 5.14)**

Recall that both bidirectional and unidirectional drivers are required. This illustration shows the typical arrangement for a bidirectional driver in a core memory system. If information is read from the cores then current in the drive line must pass through in the direction shown to generate the magnetic force. This may be an X or a Y line in the 3D and 2-1/2D memory system; or it may be a word line in the 2D system.

The read/write input activates the R source and the R sink, the address selects the individual pair desired for the selected core, and the time relationship is determined by the timing control. The current is reversed by a change in the read/write signal to activate the W source and the W sink.

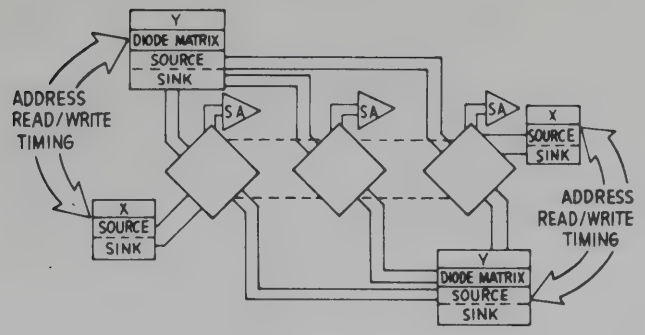



Figure 5.13. 2-1/2D Core System

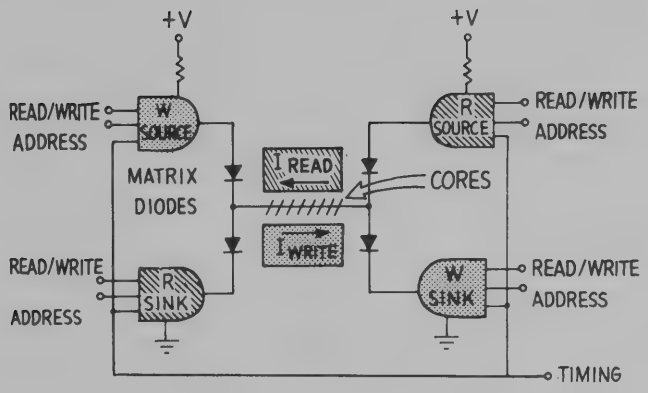



Figure 5.14. Bidirectional Driver

**Inhibit or 2D Bit Line Driver** **(Figure 5.15)**

For the inhibit driver in the 3D memory or the bit line in the 2D memory the current need flow in only one direction. For this case, the driver configuration may be as shown here. In some cases, translation of the logic control levels may be required in this source drive example because of the voltage developed across the load in the emitter.

The current requirements in these drive lines vary considerably depending on the memory size and speed requirements. In addition, core drivers must have collector-to-emitter saturation voltages below one volt at the above currents. This limits the package temperature rise due to dissipation, guarantees adequate power switched to the load and minimizes drive current variations.

Any magnetic or inductive systems usually have a reverse or counter voltage generated when the currents are changed. In a core drive system this can result in a high reverse voltage on the driver output, which means that there must be adequate limiting or voltage breakdown to prevent damage to the driver.

Another very desirable feature for a driver is that it be compatible with the low-level logic control circuitry that drives it. TTL, of course, is very popular logic and most drivers are input compatible with it.

**Monolithic Transistor Drivers** **(Figure 5.16)**

This shows two drivers that are just monolithic transistor arrays. Each contains eight N-P-N transistors. The difference is in their maximum current handling capacity and in the interconnection of the base and emitter leads. Both arrays can handle collector-to-base breakdown voltages of 25 volts. As shown, these can be used as unidirectional drivers and are selected by address decoding in these locations.

**IC Driver** **(Figure 5.17)**

This illustration shows the use of the 308 as a driver for sinking the current in a system that needs bidirectional current drive. The sink drivers are identified with a C and are used at two locations. Likewise, the diode matrices such as the TID23 are identified with a B and used at four locations.

Another type of monolithic driver, identified as A, is used for the source of the current. This driver has a dual circuit of TTL gates and a separate N-P-N transistor that can supply 300 mA of current. A discrete P-N-P is used for level shifting so that the source emitter output can be much higher (near the +V voltage) rather than just the high output of the TTL gate.

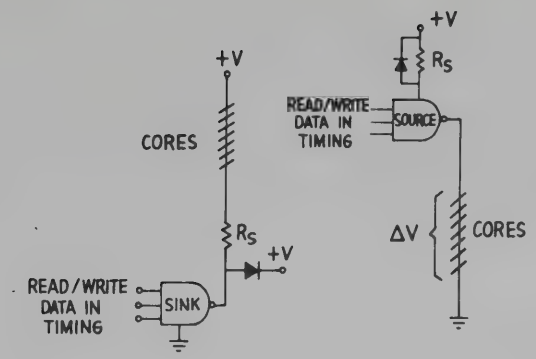



Figure 5.15. Inhibit or 2D Bit Line Driver

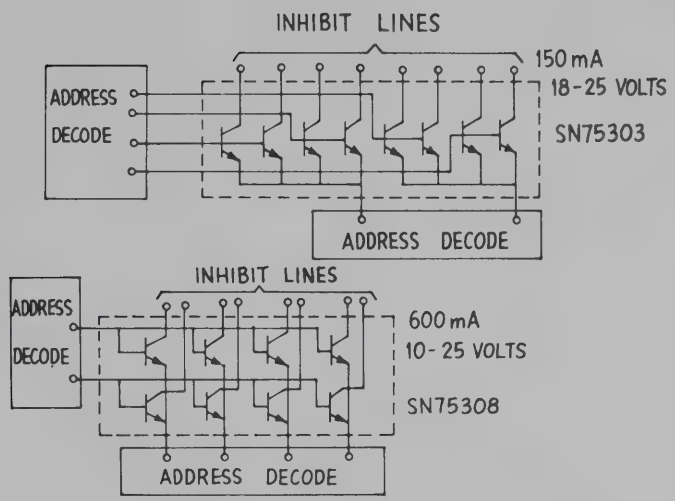



Figure 5.16. Monolithic Transistor Drivers

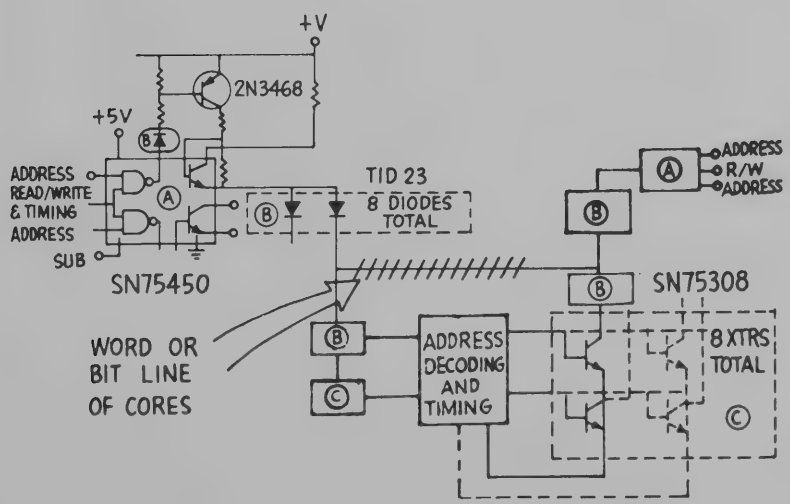



Figure 5.17. IC Driver

**Dual TTL Peripheral Drivers Product Summary** **(Figure 5.18)**

There are two complete families of these type devices as shown in Figure 5.18. In a majority of these the N-P-N output transistor has the emitter connected to ground, the collector open and the base driven by the gate output.

**SN75324** **(Figure 5.19)**

This figure has four high-speed output switching transistors controlled by seven logic inputs that are TTL compatible. Two address inputs, B and C, are used to select the source or sink mode and two address inputs are used to select the source-sink pair. There is a timing gate which has three inputs. If any one of these inputs is low, all the address gates are disabled. The sink drivers are connected in a Darlington configuration for quick response to the input signal. There are extra overdrive transistors, stack discharging resistors, and clamping diodes to protect the output transistors, limit the voltage excursions, and eliminate noise sources.

| CIRCUIT TYPE | FUNCTION* | FEATURES |
|---|---|---|
| SN75450B | AND | TWO TTL GATES AND TWO HIGH |
| SN75451B | AND | PERFORMANCE N-P-N TRANSISTORS |
| SN75452B | NAND | ON SAME CHIP |
| SN75453B | OR | $I_C$ = 300 mA |
| SN75454B | NOR | 20 V HIGH SPEED SWITCHING |
| SN75460 | AND | PIN COMPATIBLE WITH SN75450B |
| SN75461 | AND | FAMILY ABOVE |
| SN75462 | NAND | $I_C$ = 300 mA |
| SN75463 | OR | 30 V SWITCHING |
| SN75464 | NOR | SLIGHTLY SLOWER SWITCHING SPEED THAN SN75450B FAMILY |

*POSITIVE LOGIC

**Figure 5.18. Dual TTL Peripheral Drivers Product Summary**

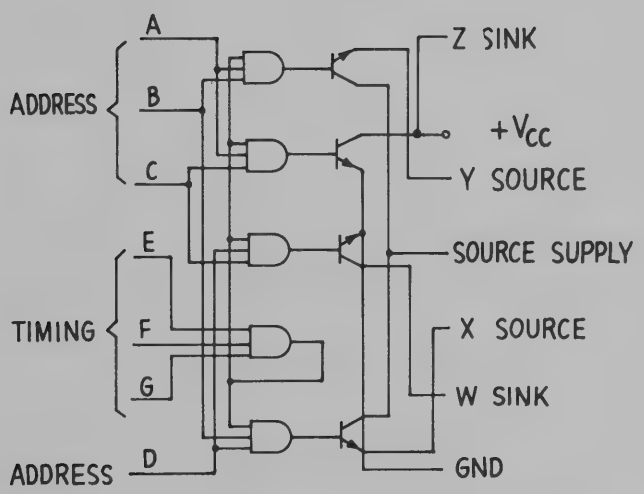



**Figure 5.19. SN75324**

**SN75324 Driver Application** **(Figure 5.20)**

This circuit applies the 324 drivers. The truth table allows more than one circuit in a package to be on at the same time but power dissipation does not permit this. With the separately packaged inverters on the address, as shown, this is prevented. Only one core line is shown in the X and Y direction. The coincident bit is in bit position E. There is a complete matrix of lines intersecting an array of cores.

The 324s and their associated inverters and resistors are identified with a C notation and are used in four locations. The A and B diode matrices are used in two places each. There is a source and sink pair at each end of the X and Y line provided by the 324s.

**SN75325** **(Figure 5.21)**

In a 2D memory system larger currents are required for the read current pulse. A monolithic unit that provides circuit capability somewhat similar to that of the 324, but can supply and sink up to 600 mA, is the SN75325, shown here.

This driver contains four output transistors capable of 600 mA current and TTL compatible gates for driving two source-switch pairs and two sink-switch pairs. Separate terminals $R_{NODE}$ and $R_{int}$ provide flexibility in setting the source current drive. For higher currents than with $R_{int}$, the appropriate resistor is connected between $V_{CC2}$ and $R_{NODE}$. This provides the advantage that the power dissipated by the resistor is external to the package.

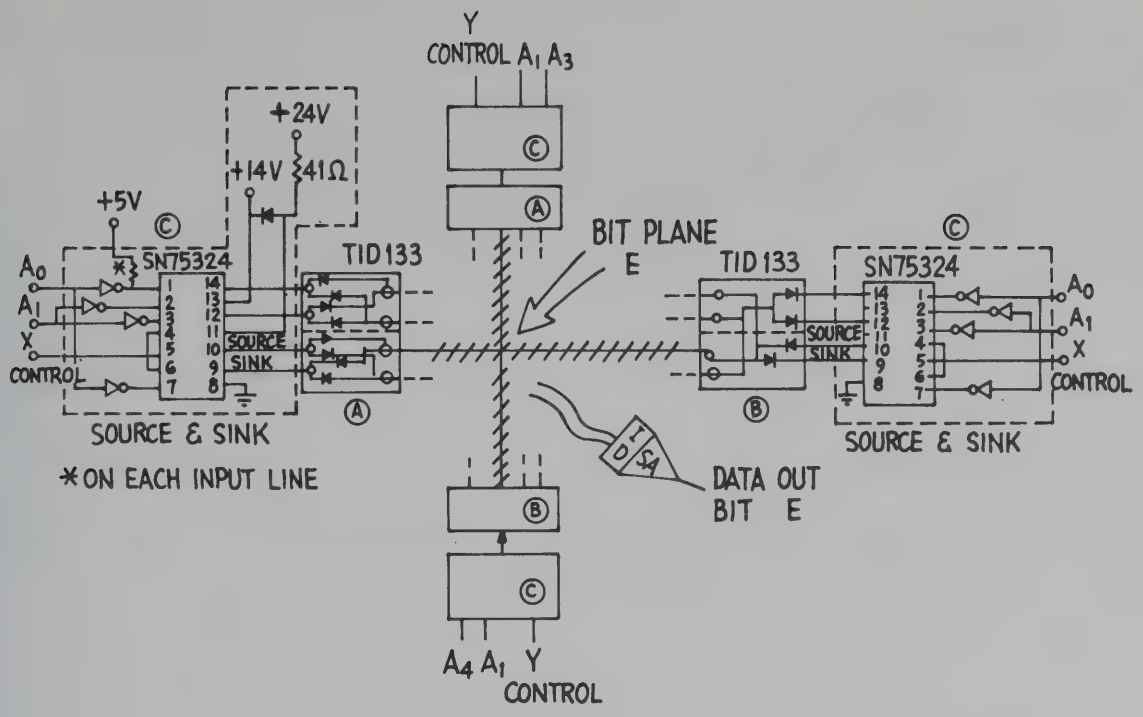



Figure 5.20. SN75324 Driver Application

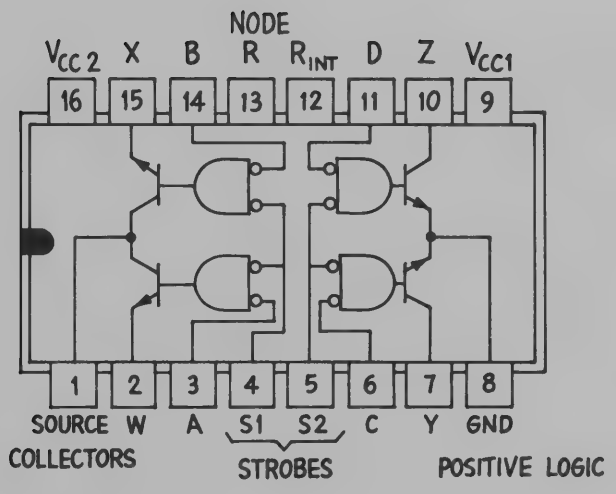



Figure 5.21. SN75325

**2D Memory Application** **(Figure 5.22)**

This is an application of a 2D memory. The word line drivers must be bidirectional with the read current greater than twice the $I_{PW}$. The bit current need only be in one direction and only of a magnitude of $I_{PN}$. Therefore, 325 drivers are used for the word lines and transistor arrays, 75308s, are used for the bit drivers. The source and sink drivers are selected by the address decode and $S_1$ and $S_2$ are used as strobes for timing the source and sink switches.

**2-1/2D Memory Application** **(Figure 5.23)**

This figure illustrates the 2-1/2D memory system. The drivers used here are 324s. The address selection is such that the same one of these $Y_0$, $Y_1$, $Y_2$, and $Y_3$ lines is selected at the same time, providing an $I_{PR}$ current for each bit. $I_{PR}$ current also flows in a selected X wire. Therefore, bits 0, 1, 2 and 3 are read out from the core matrix for four bits of this word.

## SUMMARY

This lesson has covered the characteristics of cores, how the core memory systems are organized, and the type of monolithic drivers that are used to increase performance and reduce cost. The cost reduction is primarily due to the integrated circuit and the associated packaging and assembly cost reductions. Further advances will occur for these drivers to help extend the usefulness and cost effectiveness of the core memory until the semiconductor memory takes over many of the functions.

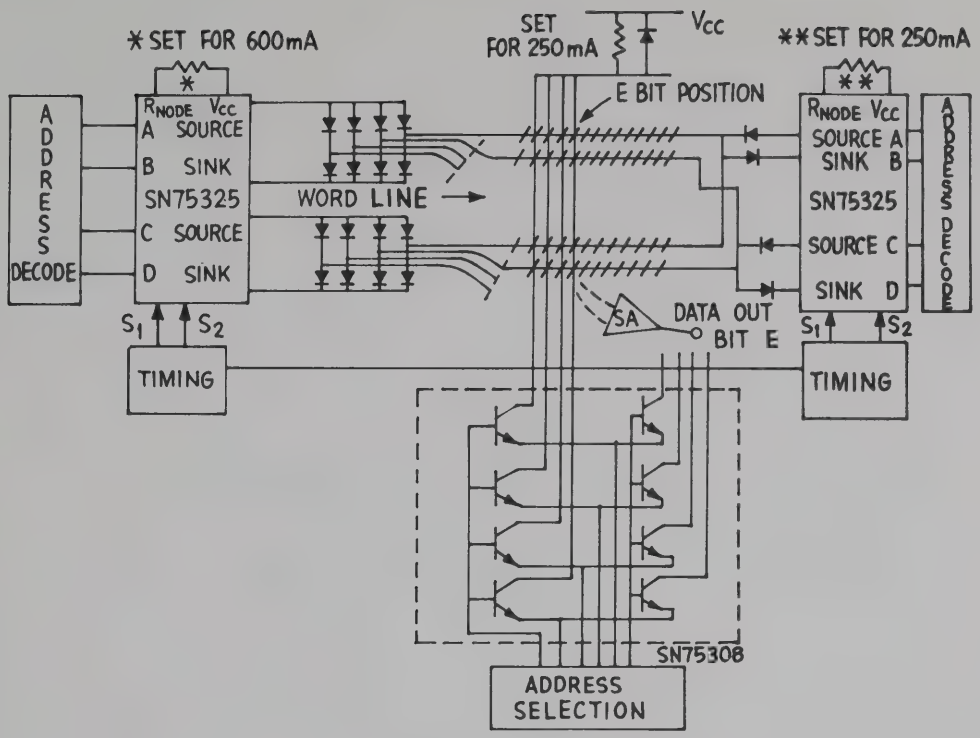



Figure 5.22. 2D Memory Application

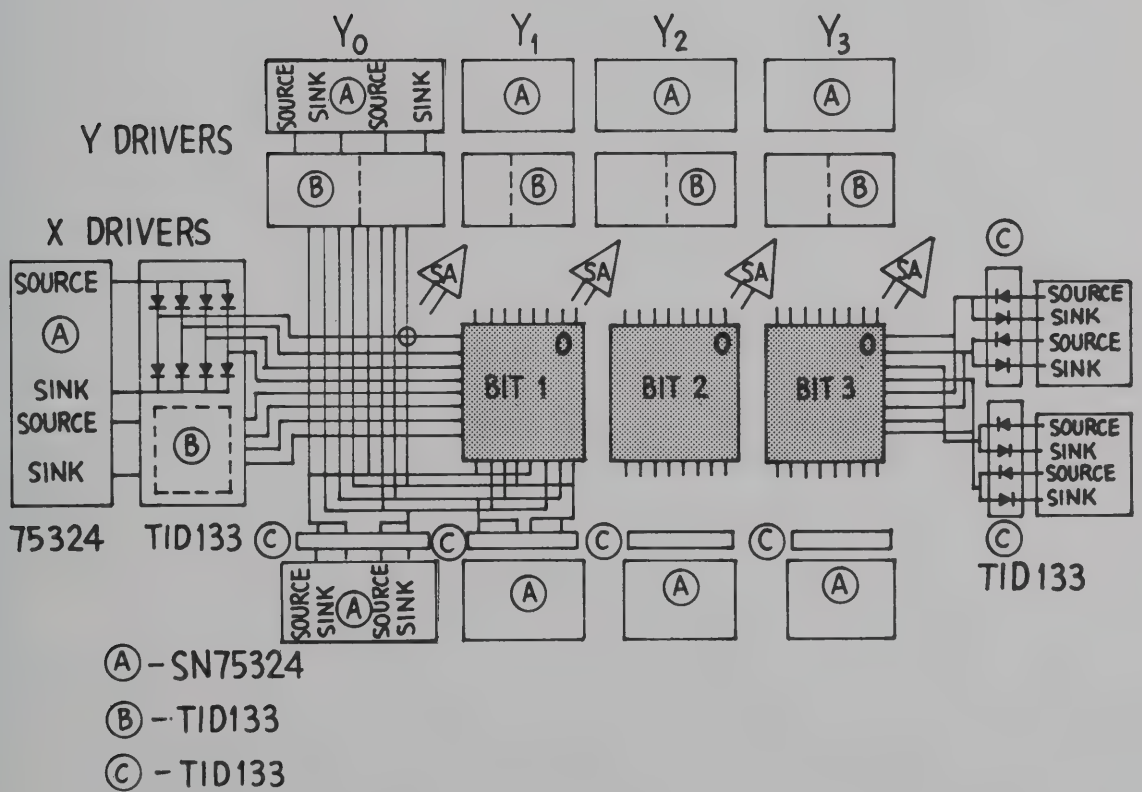



Figure 5.23. 2-1/2D Memory Application

# Lesson 6

# SEMICONDUCTOR MEMORY DRIVER APPLICATIONS

*Interface drivers for TTL and MOS memories as well as CMOS logic from TTL and ECL logic levels are described and specific applications discussed. The difference between an interface with p-channel and n-channel MOS is stressed.*

# Lesson 6

# SEMICONDUCTOR MEMORY DRIVER APPLICATIONS

*Within the family of interface integrated circuits a number of different types of translators and drivers are used. Our discussion in this session centers on so-called semiconductor memory drivers, or drivers to provide control and timing signals to semiconductor storage elements.*

*In the case of such drivers, we will find that they may translate and level shift logic levels as well as having the capability to provide large currents for charging capacitance. The latter is even a necessity for bipolar memory systems using TTL storage elements.*

**Interface Paths** **(Figure 6.1)**

As illustrated by this diagram there are a number of different interface paths: ECL to TTL, ECL to MOS, TTL to MOS and TTL to TTL. Let's begin with TTL driving TTL storage elements because it is a familiar logic system.

**Simplified Memory System** **(Figure 6.2)**

Here is a simplified memory system. The total number of storage bits in each package is organized into words, W, times the bits, B, in each word. This is called the organization.

**Simplified Memory System** **(Figure 6.3)**

For our present discussions let's consider that the organization is $W_I$ words times $B_I$ bits. $W_I$ represents the words in each package and $B_I$, the bits internal to each package contributing to forming the total bits in the word.

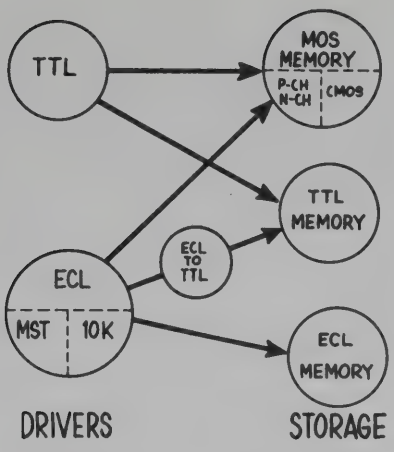



Figure 6.1 Interface Paths

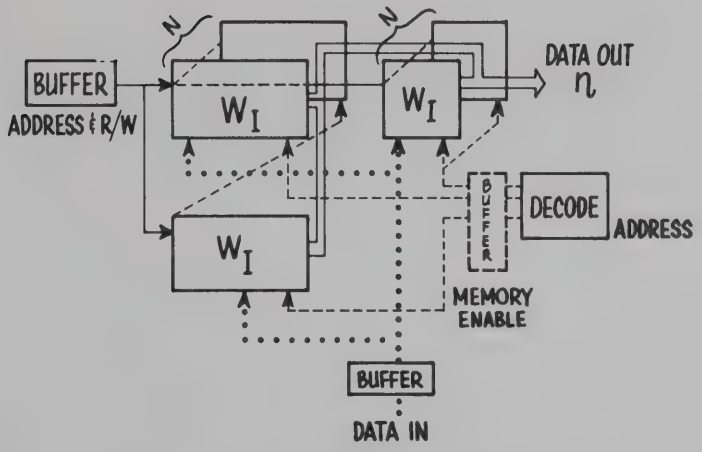



Figure 6.2. Simplified Memory System

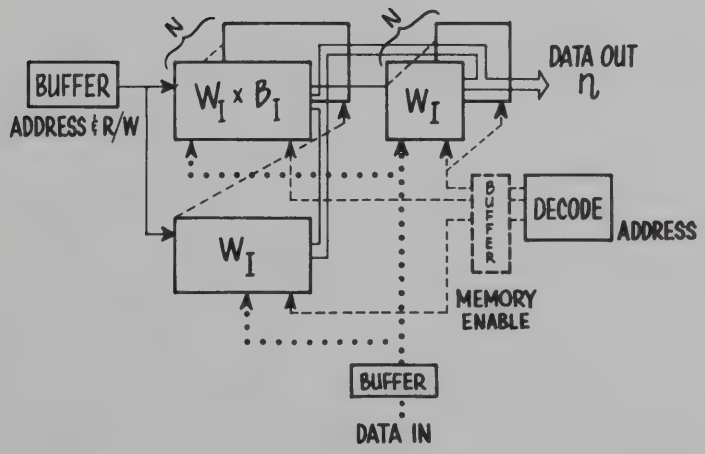



Figure 6.3. Simplified Memory System

**Simplified Memory System** **(Figure 6.4)**

For our example we will consider $B_I$ equal to 1 for an organization of $W_I$ words by one bit. Therefore, each package can be identified with $W_I$. As an example, if this is a 256-bit storage element then the organization would be 256 words by one bit.

N bits are required in each word, and these are provided by the N packages shown behind each $W_I$ package. N packages must therefore be energized simultaneously in order to store and read out all bits of a word at the same time.

**Number-of-Pages Equation** **(Figure 6.5)**

Now if we want a memory system with M words and N bits, then the number of packages required is given by the equation in this figure, where $W_M$ is the total words required and $B_N$ is the total bits per word. $W_I$ and $B_I$ are as previously described.

**Simplified Memory Systems** **(Figure 6.6)**

New drivers or buffers are required as shown in the system to program various functions in the addressing, data input and output, and decoding processes. In addition, dynamic MOS storage elements require timed (clock) signals in addition to the other signals shown. These may or may not be decoded depending on the system.

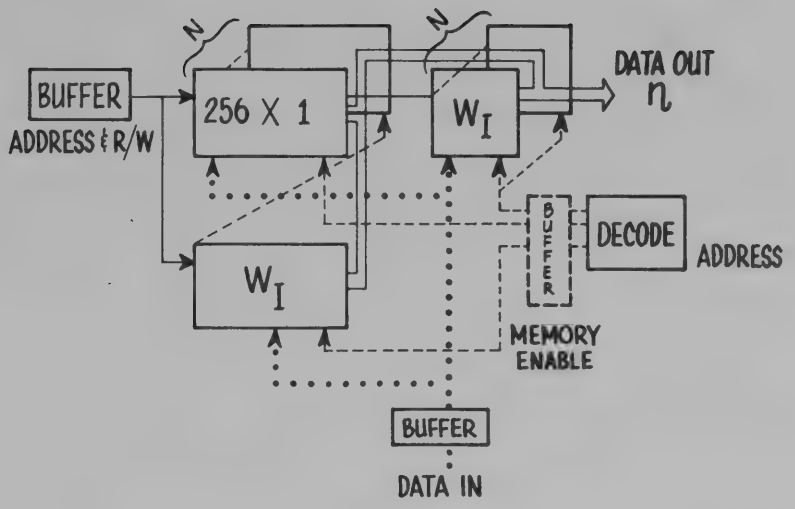



Figure 6.4. Simplified Memory System

$$\frac{W_M}{W_I} \cdot \frac{B_N}{B_I}$$

Figure 6.5. Number-of-Pages Equation

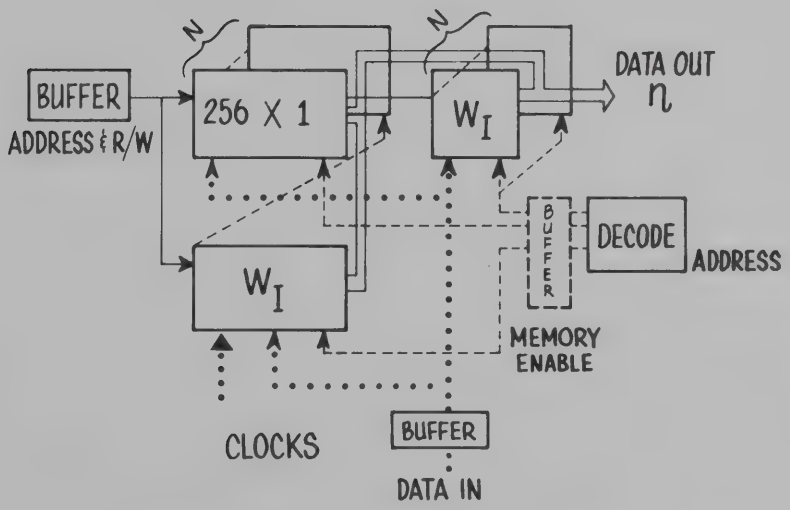



Figure 6.6. Simplified Memory System

**Load on Driver** **(Figure 6.7)**

The load on a driver that is supplying the address and read/write signal is $L_A$, which is a function of both the number of words and the number of bits. It is equal to the total words required divided by the words per package, times the total bits in a word divided by the bits in each package times the impact load factor, ILF. The number of lines to be decoded, assuming only one select or enable line per package is used, is $W_M$ over $W_I$, and the load on each of these lines is $B_N$ over $B_I$ times ILF.

Data-in lines present a load of $W_M$ over $W_I$ times the input load factor. These last two are functions of either words or bits, therefore, their loading is not going to be as large as the address line loading. Let's return to the input loading factor, ILF. The input loading factor is the load that an input line presents to the driver whether the input be to a gate, or board, or a total memory system. It may be expressed as a current, voltage, or impedance, or a combination of these.

**Input Loading Factors** **(Figure 6.8)**

This example shows input loading factors for different types of semiconductor storage elements. A standard TTL input has an ILF of −1.6 mA; the driver must provide a current sing, and a capacitance of from 2.0 to 3.0 pF. Or there are some memory elements that need only −0.5 mA sink current. If the input is a P-N-P the ILF is −0.25 mA and 1.5 to 2.5 pF and if it is ECL, ILF is +50 microamperes and 2 to 3 pF.

**ILF of MOS Inputs** **(Figure 6.9)**

As seen in this illustration, the ILF of MOS inputs has very high capacitance, from 3.5 pF to 40 pF, the latter for a precharge control or reset clock line.

ADDRESS AND READ/WRITE

$$L_A = \frac{W_M}{W_I} \cdot \frac{B_N}{B_I} \cdot ILF$$

NUMBER OF DECODER OUTPUTS

$$\text{No. OF LINES} = \frac{W_M}{W_I}$$

LOAD ON DECODED LINE

$$L_D = \frac{B_N}{B_I} \cdot ILF$$

DATA-IN

$$L_{ID} = \frac{W_M}{W_I} \cdot ILF$$

Figure 6.7. Load on Driver

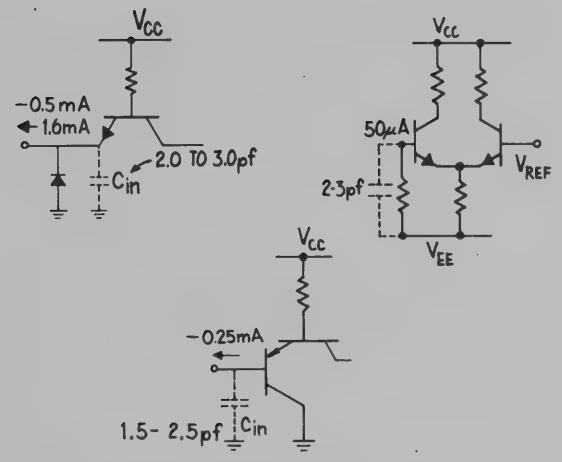



Figure 6.8. Input Loading Factors

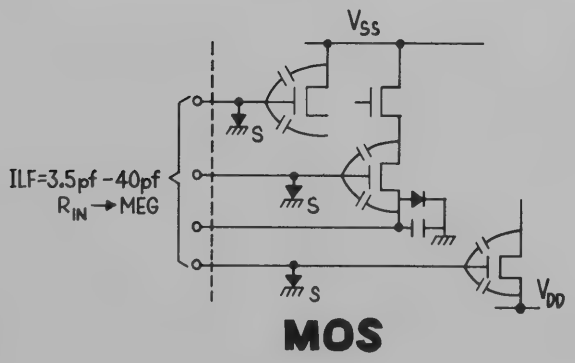



Figure 6.9. ILF of MOS Inputs

**Equation of Address Line Loading** **(Figure 6.10)**

As shown in this example, suppose our memory system required is an 8192 words by 16 bits and we use a TTL storage element with an ILF = 0.5 mA and 2.0 pF on the inputs and 1024 words by 1 bit in the package. We will work with the address line because that's the worst loading. Therefore,

$$L_A = \left[\frac{8K}{1K} \cdot \frac{16}{1}\right] \begin{matrix} \text{x } -0.5 \text{ mA} \\ \text{x } 2.0 \text{ pF} \end{matrix} = \begin{matrix} -64 \text{ mA} \\ 256 \text{ pF} \end{matrix}$$

The driver or buffer for the address lines must be able to sink 64 milliamperes. But not only that, there is a capacitive load that must be charged by the driver output to pull-up the output above the standard TTL threshold of 0.8 volt to at least 1.9 volts for safe design margin. Now, sinking the current is not the problem with respect to response time, because of the low impedance discharge path. It is charging the capacitance on the line to the required voltage in a given amount of time.

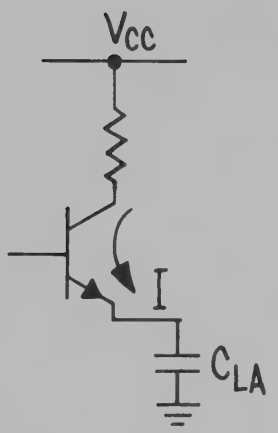
**Average Charging Current and Response Time** **(Figure 6.11)**

Parallel SN7433 or SN7438 open collector units could be chosen for this job, but an active pull-up would be better. For example, Figure 6.11 shows an active device charging the capacitor. The current I is determined by the characteristics of the active pull-up transistor, that is, its current gain and output impedance.

8,192 WORDS × 16 BITS
TTL WITH ILF = -0.5mA & 2.0pF
WITH 1,024 WORDS × 1 BIT

$$L_A = \left(\frac{8K}{1K} \cdot \frac{16}{1}\right) \times 0.5mA \times 2.0pF = \begin{matrix} -64mA \\ 256pF \end{matrix}$$

**Figure 6.10. Equation of Address Line Loading**




$$\Delta t = C_{LA} \frac{\Delta V}{I}$$

$$\Delta t = \frac{250 \times 10^{-12} \times 1.5}{25 \times 10^{-9}} = 15ns$$

**Figure 6.11. Average Charging Current and Response Time**

**High-Speed TTL Drivers** **(Figure 6.12)**

Even faster times can be obtained by using an SN74128 or the SN74S140. Figure 6.12 shows such TTL drivers.

**TTL Drivers** **(Figure 6.13)**

This illustrates how these drivers are used in a system. Included are an 8K X 16 memory system board with 128 1K bipolar TTL storage elements as the semiconductor memory and address drivers with SN74S140s used to drive the 10 address lines and the read/write line. Circled numbers represent the milliamperes of sink current required at the various driver inputs and outputs.

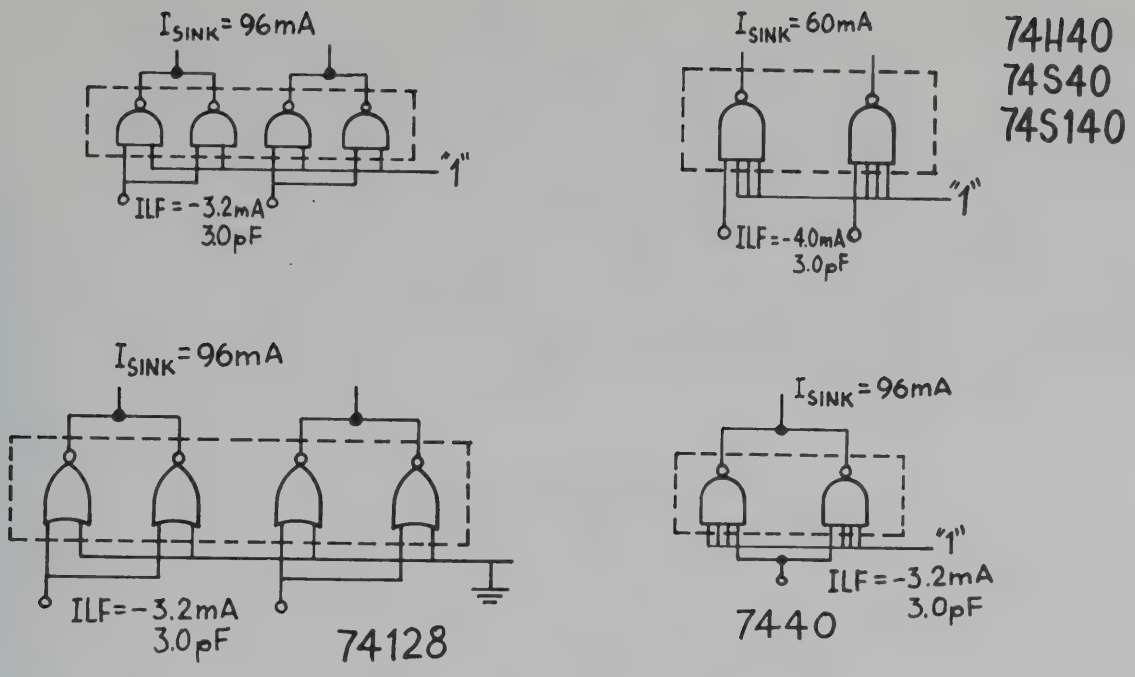



Figure 6.12. High-Speed TTL Drivers

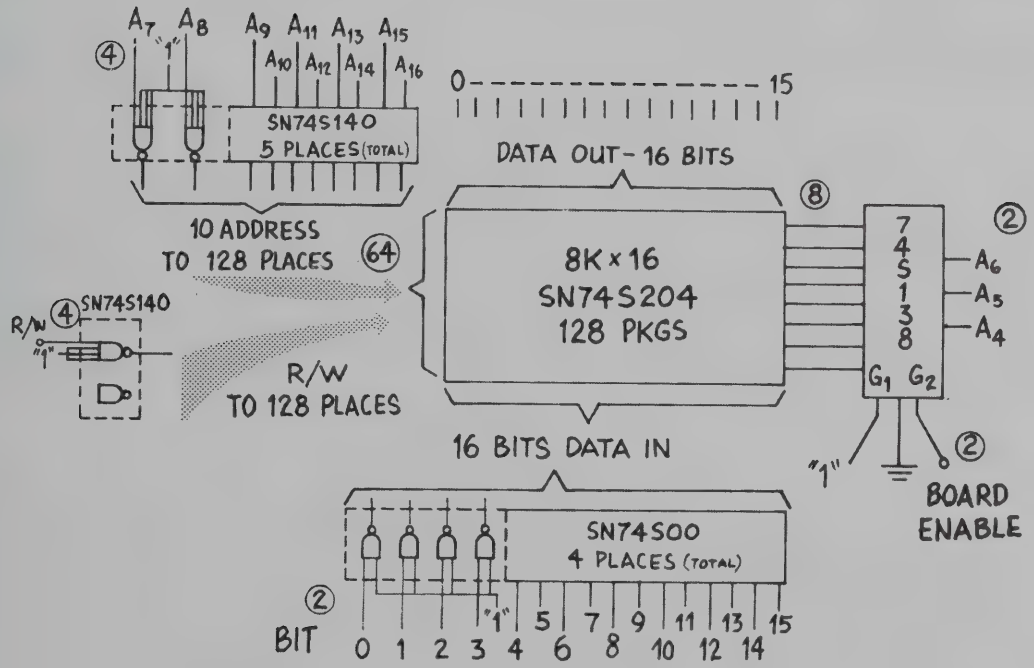



Figure 6.13. TTL Drivers

**TTL-to-MOS Interface** **(Figure 6.14)**

This illustrates a typical driver providing the address signal to a p-channel MOS storage element. The total capacitance on the line is $C_I$. The p-channel storage element has a voltage supplied with $V_{SS}$ and $V_{DD}$. $V_{DD}$ is negative with respect to $V_{SS}$. Note that the p-channel MOS device is off when the N-P-N bipolar driver output is high or near $V_{SS}$, and it is on when the driver output is low or near $V_{DD}$. More and more MOS storage elements have inputs that are TTL logic level compatible with only a clock line that must be driven with a high voltage signal. Most earlier MOS storage elements required a high voltage swing on all inputs. We will deal first with the high voltage driver.

**Voltage Supply** **(Figure 6.15)**

The output swing is from 10 to 20 volts as shown in this drawing. The levels of the swing must be controlled within limits. The high level must not go above $V_{IHA}$; otherwise carriers will be injected into the substrate and the data destroyed. In like fashion, the signal level must be $V_{IHB}$ to make sure the p-channel MOS gate-to-source voltage is less than a threshold voltage $V_T$, and the device is off. The low level must at least be down to $V_{ILA}$ to get the correct speed of turn-off and above $V_{ILB}$, otherwise a breakdown or a field oxide voltage may be exceeded. Now, for p-channel MOS storage elements, the idle or standby state is when the input is near $V_{SS}$ because the devices are off. Fortunately, this is also the low dissipation state of the N-P-N bipolar drive when the output is near $V_{SS}$. High standby power, greater than 10 to 1, is dissipated when the driver output is low, near $V_{DD}$.

**MOS Storage Elements** **(Figure 6.16)**

This shows an n-channel MOS storage element. The situation is somewhat different. $V_{DD}$ is a positive voltage with respect to $V_{SS}$. The n-channel device in the storage element has its source connected to $V_{SS}$ and its gate voltage must be near $V_{SS}$, less than a $V_T$, to turn off the MOS device. Therefore, if an N-P-N bipolar driver is used, the output voltage is at the low level when the n-channel device is off. Therefore, the drivers are dissipating high power while the n-channel MOS is in the low standby condition. This calls for special techniques to reduce the power dissipation during the time that the storage element is in standby or not enabled.

**N-Channel MOS** **(Figure 6.17)**

One simple technique is to add a discrete P-N-P transistor between the driver output and the n-channel storage element as shown in this illustration. The high level for the N-P-N driver is now a low level to the n-channel MOS. As with the open collector TTL driver, the response time is limited by the pull-down resistor and the line capacitance time constant.

| INPUT LOGIC LEVEL | $V_O$ VALUE | STATE OF P-CHANNEL GATE |
|---|---|---|
| $V_{OH}$ | NEAR $V_{SS}$ | OFF |
| $V_{OL}$ | NEAR $V_{DD}$ | ON |

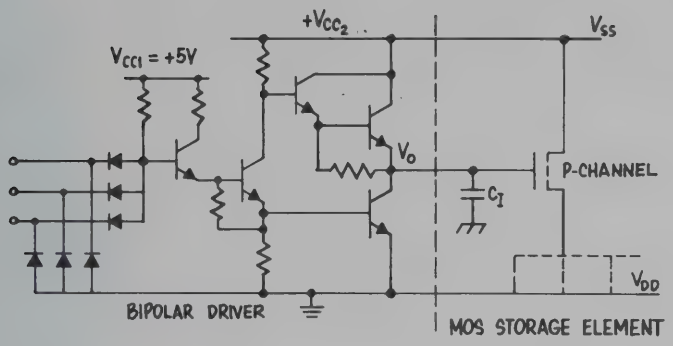



Figure 6.14. TTL-to-MOS Interface

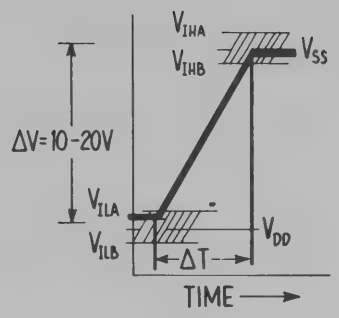



Figure 6.15. Voltage Supply

| INPUT LOGIC LEVEL | $V_O$ VALUE | STATE OF N-CHANNEL GATE |
|---|---|---|
| $V_{OH}$ | NEAR $V_{DD}$ | ON |
| $V_{OL}$ | NEAR $V_{SS}$ | OFF |

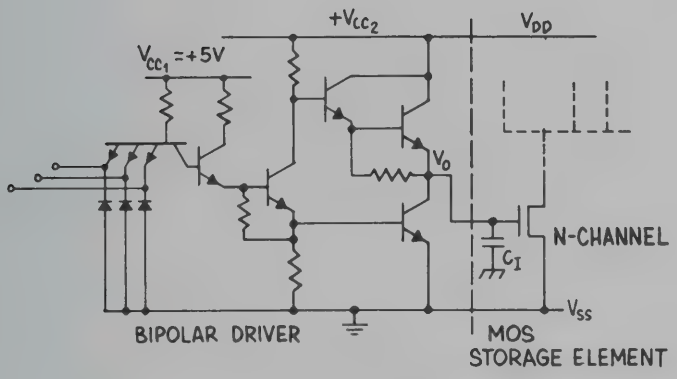



Figure 6.16. MOS Storage Elements

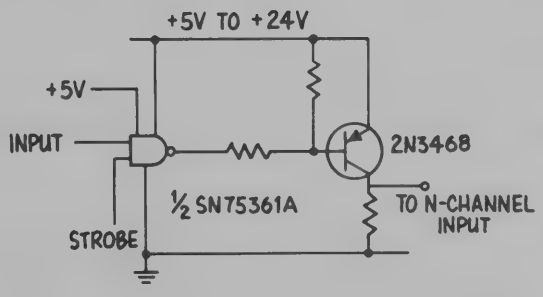



Figure 6.17. N-Channel MOS

**Power Dissipation** **(Figure 6.18)**

Little power is dissipated in the capacitor but significant power is dissipated in the driver during this time. It is equal to $CV^2f$, the total capacitance driven times the voltage swing squared, times the frequency at which the voltage levels are changed. This power must be added to the normal operating power of the driver and must be included in calculating the heat exchange cooling for the memory system.

**MOS Memory System** **(Figure 6.19)**

This illustration shows an 8K by 16 bit MOS memory system with only the address drivers shown. The address line loading is 896 picofarads because each address line of the 1K 1103 storage element has 7 picofarads of capacitance. The driver chosen for this application must be able to supply a swing of 16 volts from ground of $V_{DD}$ to +16 volts $V_{SS}$, one of them for each of the 10 address lines. Also, fast propagation delays, because the delay through the buffers, contribute to system access time. To maintain propagation delays at approximately 40 nanoseconds, the load on each driver will be limited to 4K X 16 or 448 pF. Examining such a driver in detail, the input to such drivers is from register, control circuitry, or other support circuitry that is operated with low-level logic. Therefore, a translation must occur from this low-level logic to the high voltage drive required. Previously, discrete components or a combination of discrete components and integrated circuits has been used to solve this interface drive. Now, however, monolithic drivers are available for this purpose.

**Operation of TTL Inputs** **(Figure 6.20)**

In this SN75361A driver, the TTL inputs operate at standard +5 volts. $V_{CC1}$ and $V_{SS}$, which is another $V_{CC}$, can be any voltage from 4.75 volts to 24 volts. Thus it provides the TTL to MOS voltage translation and is designed for high charging currents at fast speed and compatible 8-pin dual-in-line packaging. Recall that we talked about special techniques to lower the n-channel driver power dissipation when the storage element is not enabled. Let's examine this further.

**Output Stage of 362-Type Driver** **(Figure 6.21)**

This shows a modified output stage of the 361A-type driver. The resistor drive, which used to be connected to the $V_{SS}$ terminal, is brought out separately and the strobe terminal sacrificed. This means that the collector voltage of transistor $Q_1$ can be turned off. This now is an SN75362 driver. With $Q_1$ on, $Q_2$ is on. The collector of $Q_1$ would normally be pulled low to keep $Q_3$ and $Q_4$ off. Thus, $V_o$ would be at the low-level and a high amount of power is dissipated in $R_C$. To eliminate this dissipation when the output drive line is to be low (off mode of n-channel MOS) the $V_{BB}$ voltage is switched off.

$CV^2f$

C=TOTAL CAPACITANCE DRIVEN
V=VOLTAGE SWING
f=REPETITION RATE OF VOLTAGE SWING

Figure 6.18. Power Dissipation

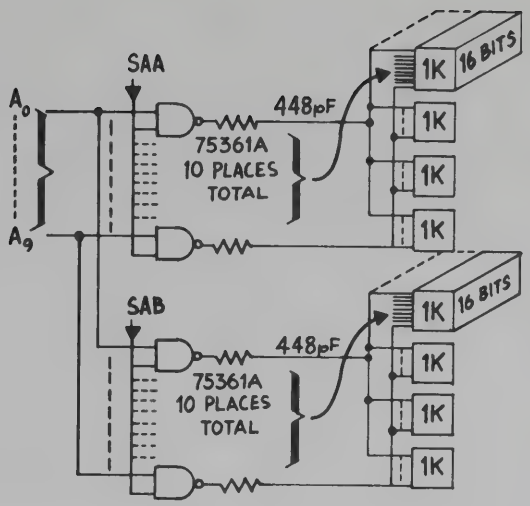



Figure 6.19. MOS Memory System

- PROVIDES GOOD UP-LEVEL FOR MOS "TTL COMPATIBLE" INPUTS
- HIGH CHARGING CURRENTS
- USE AS TTL DRIVER

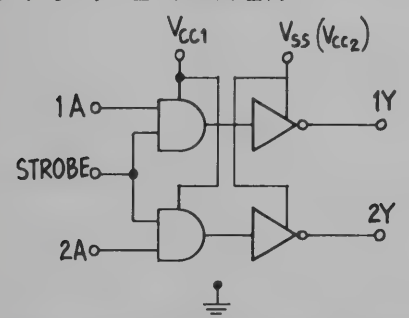



Figure 6.20. Operation of TTL Inputs

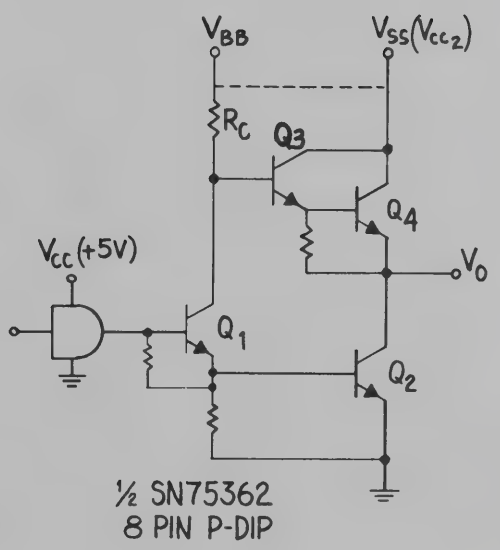



Figure 6.21. Output Stage of 362-Type Driver

**Application Technique for 362** **(Figure 6.22)**

This shows an application of that technique when a 362 is used as an address or clock driver. The $V_{SS}$ voltage is constant and of the value necessary to meet the n-channel drive requirements. $V_{BB}$ is gated through this P-N-P discrete device driven by a 361 driver from TTL levels. $V_{BB}$ is at least the same voltage as $V_{SS}$, but it could be higher to make the output even closer to $V_{SS}$. The 361 can be controlled by the enable signal, either board enable or chip enable, to turn on $V_{BB}$ to the 362 through the P-N-P transistor only during the time the storage elements receiving the address signal are enabled. This saves 66% of the power dissipated when the 362 is in the low level. Considerably more power, another 29%, can be eliminated by also gating the +5 V line to the 362 drivers. The input stages are also gated through a P-N-P transistor by a simple TTL gate controlled by the enable signal. Resistors $R_2$ must be added to the output line of the driver for this case to discharge the MOS address line to ground when the supplies are disengaged. $R_1$, of course, is to prevent ringing.

**List of Types and Their Applications** **(Figure 6.23)**

There are a wide variety of these types that have basically the same output stage.

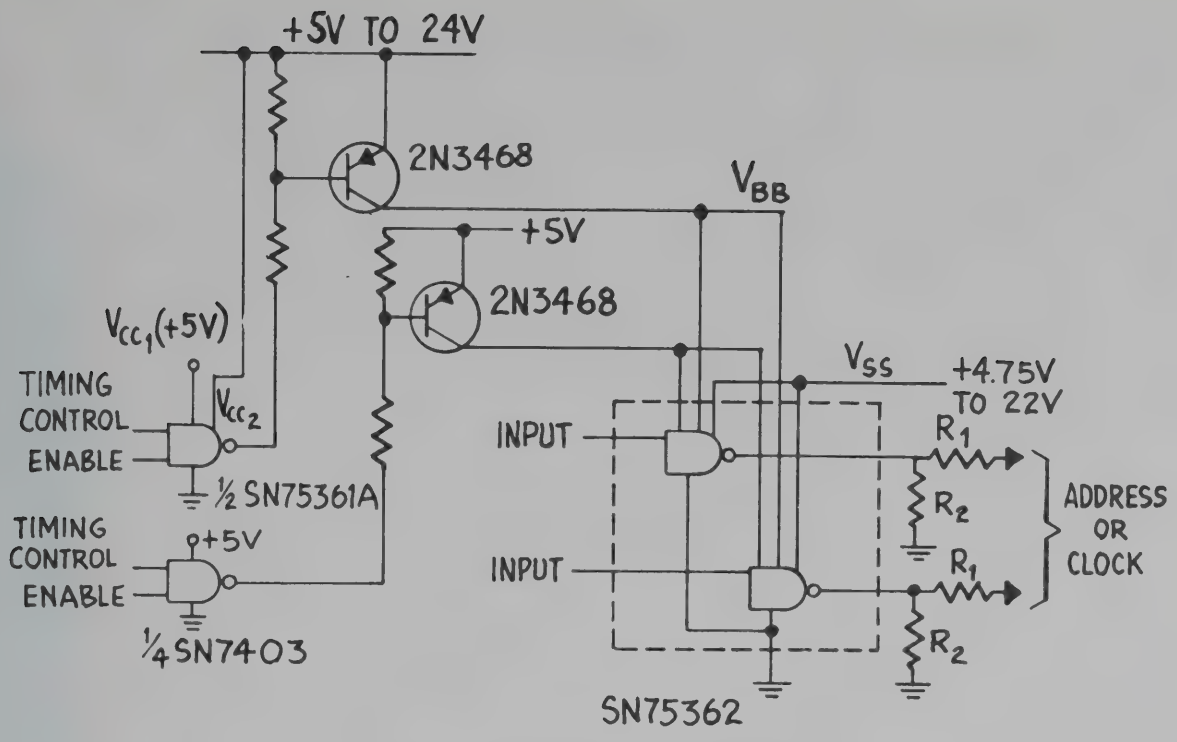



Figure 6.22. Application Technique for 362

| CIRCUIT | TYPE | FUNCTION | $V_{SS}$ (MAX) | $V_{BB}$ | PACKAGE |
|---|---|---|---|---|---|
| *360 | DUAL | TTL-MOS | +12 | NO | 8 P |
| 361A | DUAL | TTL-MOS | +24 | NO | 8 P, N |
| 362 | DUAL | TTL-MOS | +24 | YES | 8 P |
| 363 | DUAL | TTL-MOS | +15V | NO | 8, 16 N |
| 367 | QUAD | TTL-CMOS (TRI-STATE) | +12V | OPTION | 16 N, J |
| 368 | DUAL | ECL-MOS | +24V | YES | 14 N, J |
| 369 | DUAL | MOS CLOCK DRIVER(6003) | +5V TO-15V | NO | 8 P |
| 370 | DUAL | READ/WRITE & SA (4062) 6002 | +24V | NO | 16 N, J |

*SN75---

Figure 6.23. List of Types and Their Applications

**Simplified Diagrams for 1103 and 4062 MOS Memories (Figures 6.24 and 6.25)**

These are simplified diagrams of the use of these devices for the 1103 and 4062 1K p-channel dynamic MOS memories. The address read-write, precharge, chip enable clock signals X and R/W can all use the 361A family. The 1103 signals are 20 volts. Data-in must be a high voltage for the 1103 X while it is a TTL level into the special monolithic writer driver and sense amplifier, the SN75370. The TTL compatibility of MOS storage elements has generally simplified the interface driver problem because of the common +5 V power supply. However, high voltage clocks must still be used and some of these must be displaced or driven between a plus and a minus voltage.

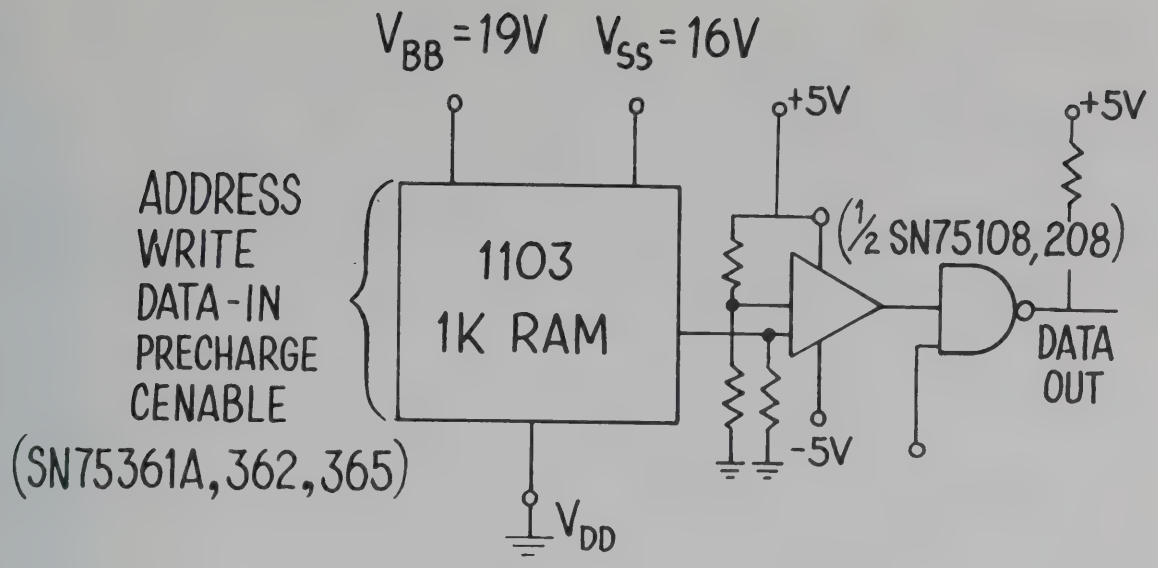



Figure 6.24. Simplified Diagram for 1103 MOS Memory

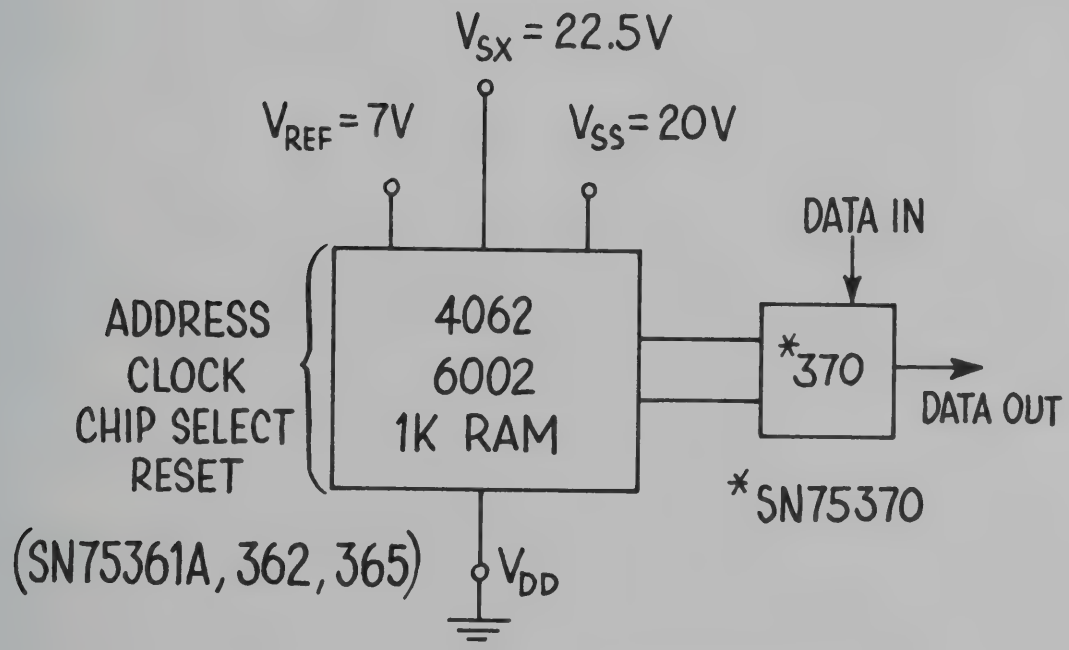



Figure 6.25. Simplified Diagram for 4062 MOS Memory

**2K P-Channel Dynamic RAM** **(Figure 6.26)**

Such an application is shown in this illustration. A 2K p-channel dynamic RAM, the 6003, is used. Three clocks must swing between +5 V and −15 V, and the 369, which has dual circuits in a package, is used especially for this purpose. The inputs must be translated from TTL levels down to TTL levels referenced to −15 volts and a discrete P-N-P is used for this. A 361 driver is used on the eleven address lines, one chip select, one write enable, and one data in line because the "so-called" TTL compatible inputs need a high level of 3.5 volts.

**N-Channel MOS Storage Element** **(Figure 6.27)**

This demonstrates the use of the 368 in a typical memory interface for the 7001. This is a 1K dynamic n-channel MOS storage element that essentially has the characteristics of a static MOS storage element because it uses a charge pump refresh, first described by Burke and Michon of General Electric at the 1972 Solid State Circuits Conference. It has an access time of 55 nanoseconds without the sense amplifiers and translation circuitry. A somewhat similar speed device is the 1500 and the 2105 which need one pulse per cycle for what is called a transparent refresh rather than the periodic refresh of previous dynamic storage elements. We've discussed TTL to TTL, TTL to n- and p-channel MOS and ECL to n-channel MOS. The only problem path remaining is the TTL to CMOS path. It is filled with a quad driver that again is the same type as the 361A family except it has a +12 volt swing and a tri-state output with a disable input on each gate rather than a common strobe. It is identified as the SN75367 in the 16-pin plastic package. Again the output is capable of high drive currents and fast speed performance.

## SUMMARY

The drivers discussed work equally well for driving the address lines of fixed program memory (ROMs and PROMs) or sequentially accessed memory (shift registers). Significant strides have been made to provide high-current capacity drivers in a small package. Further developments with Schottky designs will keep advancing the product family in the future.

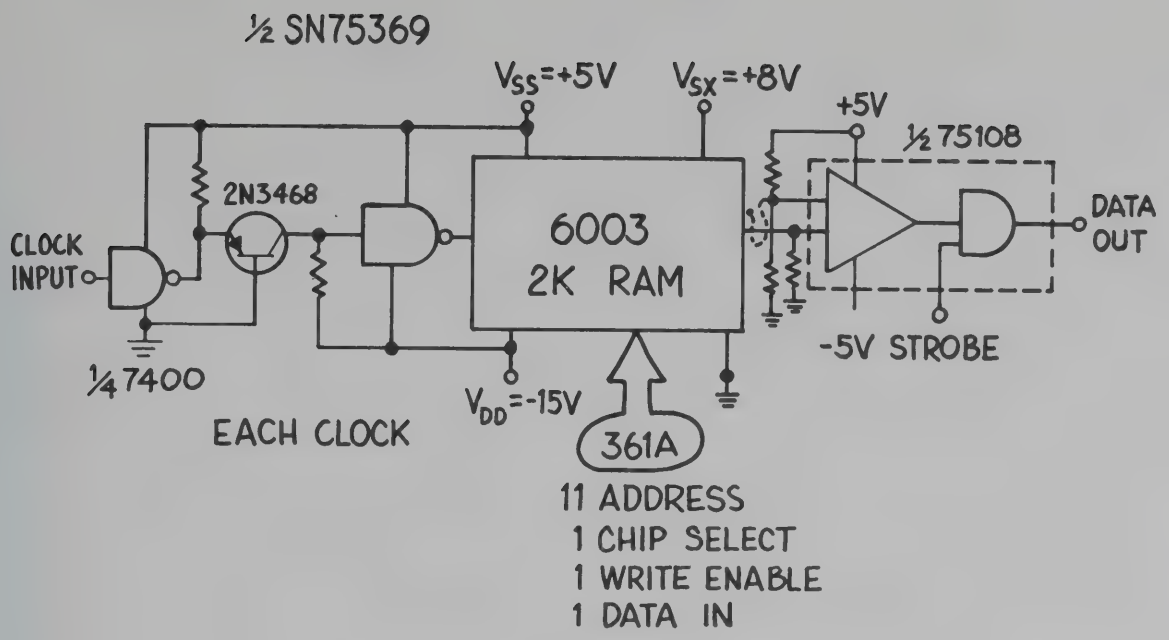



Figure 6.26. 2K P-Channel Dynamic RAM

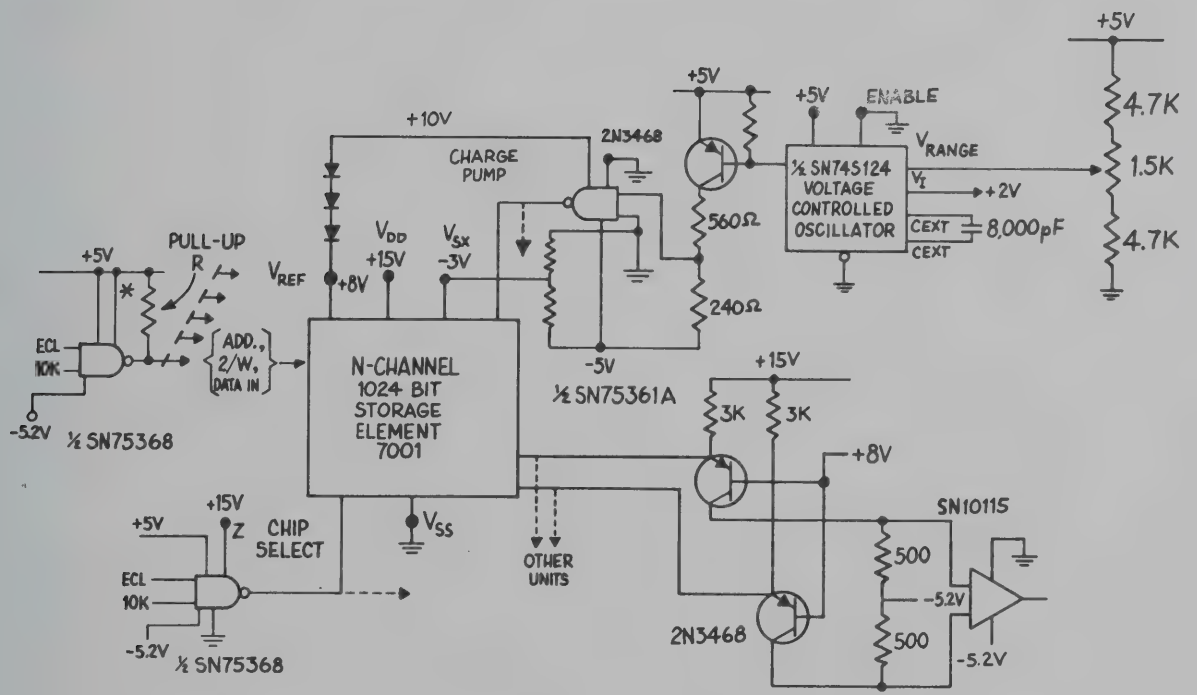



Figure 6.27. N-Channel MOS Storage Element

# Lesson 7

# SENSE AMPLIFIERS

*Basic requirements are established and characteristics defined. System applications and variations in performance are discussed for a core memory and MOS memory system. Direction is given to other similar applications.*

# Lesson 7

# SENSE AMPLIFIERS

*Basically, the sense amplifier can be considered as an accurate fast threshold detector with a strobing or gating capability and usually with an output that is easily connected to achieve pulse stretching requirements. Such a versatile circuit finds application not only in the reading of core or other memories but in the areas of line receivers, digital telemetry, and a wide variety of other signal processing tasks.*

**Digital "0" and "1" Level Signals** **(Figure 7.1)**

The basic application of the sense amplifier is the discrimination between a "0" and a "1" signal on a given line in some memory or digital communication systems. In all such cases the "0" and "1" signal levels tend to vary in magnitude due to the variability in source amplitudes as well as the random effect of system noise on the signal strength. As a result, the signal being received may look like the one shown with the possibility of positive or negative "1" signals and the problem faced by the sense amplifier is to decide whether the signal being received is an "0" or a "1." In order to achieve 0% error rate in this decision process we need a threshold detector that examines the magnitude of the input signal regardless of polarity and we must adjust the threshold of this element so that it is above the highest "0" level voltage magnitude but below the lowest possible "1" level voltage magnitude.

**Basic Components of a Sense Amplifier** **(Figure 7.2)**

The input amplifier and the threshold element are generally differential emitter coupled pair amplifiers and may be combined in the same circuit. These circuits have the advantages of high sensitivity, high common-mode rejection, accurate threshold control, and fast recovery from input overloads. In integrated form they also can offer excellent temperature stability in threshold and offset parameters.

**Detection Thresholds** **(Figure 7.3)**

Again, since the amplifier-threshold detector circuitry must accept both positive and negative signals, the threshold circuitry must take the form of a dual comparator to provide a transfer function of this type. Here thresholds occur at $+V_T$ and at $-V_T$ to perform the same threshold detection on positive and negative signals.

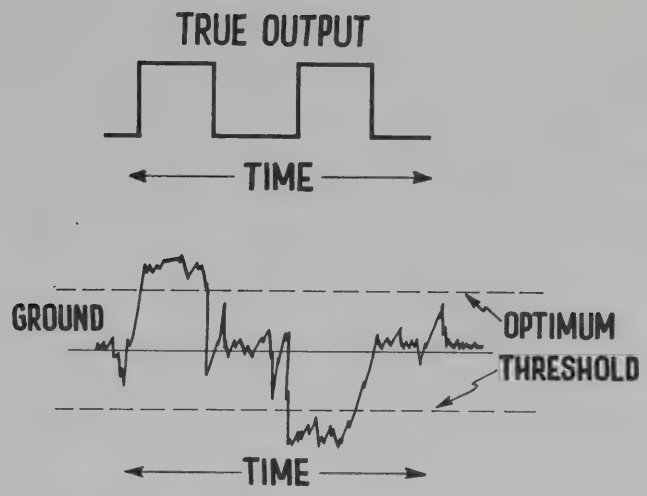



Figure 7.1. Digital "0" and "1" Level Signals

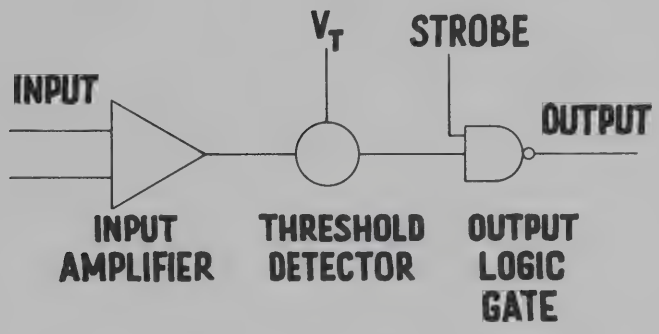



Figure 7.2. Basic Components of a Sense Amplifier

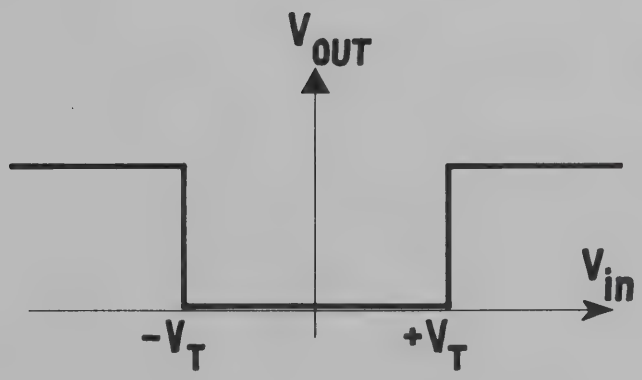



Figure 7.3. Detection Thresholds

**Transfer Characteristics of a Threshold Detector** **(Figure 7.4)**

One of the critical parameters of the threshold detector portion of the sense amplifier is the input offset voltage, which is the dc voltage that must be applied between the input terminals to force the output voltage to a specified level. In general, we can see the device characteristics that effect the input offset voltage from the general device transfer characteristics shown here. This plot shows only the actual transfer characteristics for positive signals. The curve would also apply to negative signals since the abscissa is the absolute value of the input voltage. In the actual device characteristics, the effects of finite gain on the slope of the transfer function and the variation of the characteristics over the temperature range cause the threshold to vary over a narrow range of voltages so that we have not a threshold level as such but a threshold voltage range.

**Aspects of Signal Detection** **(Figure 7.5)**

The effect of this uncertainty in the threshold in the detection process can be seen by looking at the typical "0" and "1" signals encountered in core memory operation. There are two aspects of the signal detection problem illustrated. First, for a given threshold, there are times during which even a "1" signal is below the threshold. And unless we examine the signal only during the detection window, we will not get a reliable detection of the presence of a "1" signal. The second aspect of the signal detection problem concerns the amplitude domain. Not only is there an uncertainty in the detection threshold, but the sources will vary in the "0" and "1" signal amplitudes they generate and the receiver signal amplitude will be even more uncertain due to the presence of system noise. The only solution that can be used to provide reliable "0" – "1" discrimination is to use a threshold detector that has a sufficiently narrow threshold range over the temperature range of interest or to amplify the core signals with a video amplifier before sending them to the threshold detector.

**Effect of Amplification on the Signal** **(Figure 7.6)**

The effect of amplification is shown in this drawing where now the 8 millivolt threshold range offers quite good "0" and "1" noise margins and allows for considerable core to core variability before unreliable detection can occur. Whether or not such preamplification is required for reliable system operation can be determined only as a result of extensive core characterization. If the core characterization shows that a given simple comparator could be used as the sense amplifier without preamplification, this would seem to be the most economical and simplest approach. The problem that occurs is that we need our sense amplifier to exhibit a high common mode rejection, which implies equal impedance at both comparator input terminals. Such a requirement would not be met if we connected a voltage supply directly to the inputs. Thus a relatively complex resistive voltage divider network must be used to provide the threshold voltage.

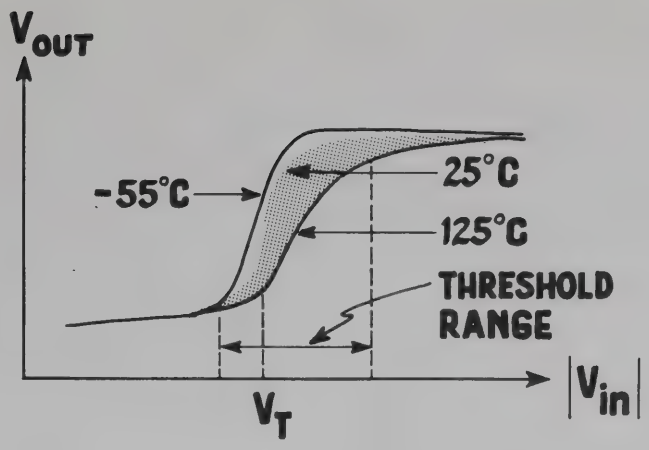



Figure 7.4. Transfer Characteristics of a Threshold Detector

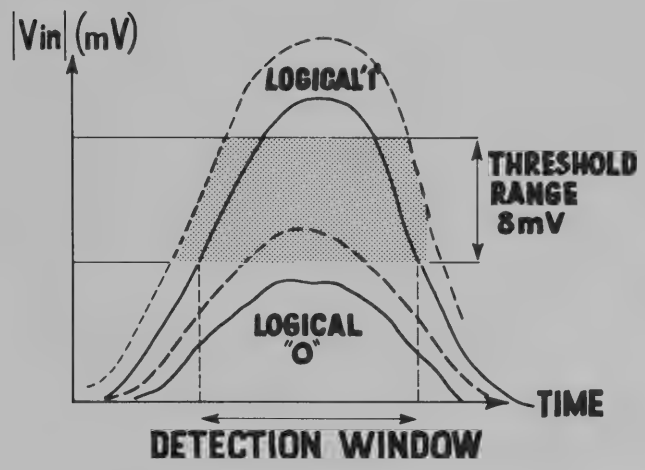



Figure 7.5. Aspects of Signal Detection

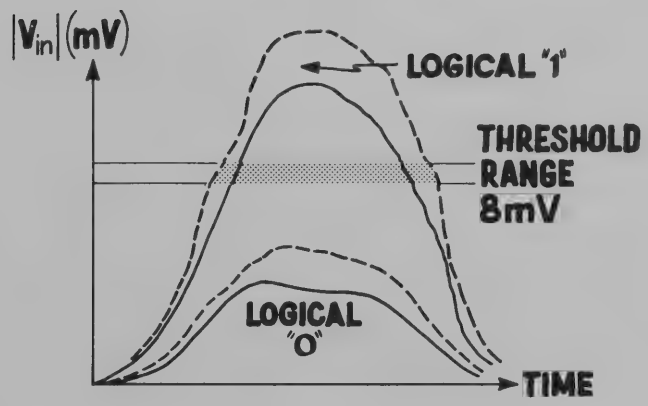



Figure 7.6. Effect of Amplification on the Signal

**Dual Comparator with an Input Resistor Network** **(Figure 7.7)**

The configuration commonly employed is to use a dual comparator with an input resistor network as shown. The dual comparator offers several advantages over the single comparator in these applications since it allows a constant threshold to be determined by well matched external resistors and allows the threshold to be individually adjusted optimally for each memory bank. The input resistor network is a simple balanced bridge which provides the same resistance to ground along any of the four paths. Thus any common-mode signal will appear equally at each comparator input and will be rejected. Other divider ratios could be used, as long as the network presents a balanced resistor configuration.

**Simplified Equivalent Circuit of Dual Comparator with an Input Resistor Network** **(Figure 7.8)**

In order to see the importance of this, let us look at the simplified equivalent circuit. In this diagram the equivalent line resistances to ground are shown as $R_{T1}$ and $R_{T2}$. These resistors provide a matched termination for the sense line as well as providing a path for the input bias current $I_B$. These resistors produce voltages from the input bias current $I_B$, from the current $I_C$ produced through stray capacitance coupling to adjacent system lines such as strobe lines, and from the offset currents $I_0$. If $R_{T1}$ is not equal to $R_{T2}$ the input bias current will generate an input voltage of $(R_{T1} - R_{T2})\, I_B$ that will act as a component of threshold offset and increase the uncertainty in the device sense amplifier threshold. Even if $R_{T1} = R_{T2}$ are very large, the differential current $I_o/2$ that flows will similarly shift the input differential voltage by an amount of $R_T I_o$. Further, if a stray coupling capacitance of C exists, a current of $C\Delta V/\Delta t$ will be generated and a $\Delta V_T$ of $C\,(R_{T1} - R_{T2})\,\Delta V/\Delta t$ will be generated.

**An Example Showing Effect on Signal** **(Figure 7.9)**

An example problem will indicate the magnitudes we might typically encounter. If the $R_{T1}$ and $R_{T2}$ are mismatched by 10 ohms and are nominally 100 ohms with the SN72711 bias current of 25 microamperes and offset current of 0.5 microampere, the effect of the bias current on the threshold would be a 1/4 millivolt change and the offset current effect would be a 1/20 millivolt change. For a line-to-line coupling capacitance of 2 pF and a signal on the adjacent line of 3 volts with a 10 nanosecond rise time, the capacitive coupling would induce a 6 millivolt signal which could cause an error in the "1" comparator output. Thus, to prevent parasitics from generating system errors we should keep $R_T$ small, closely match $R_{T1}$ and $R_{T2}$ and minimize C to avoid increasing the threshold uncertainty or thus increasing the detection errors.

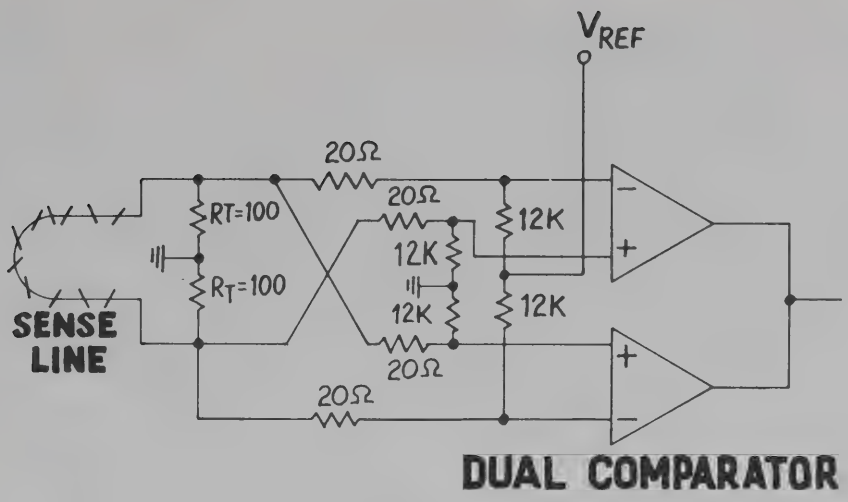
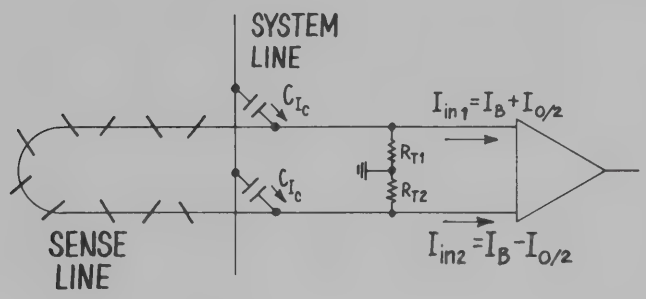



Figure 7.7. Dual Comparator with an Input Resistor Network




$$I_O << I_B \quad \text{IF } R_{T_1} \neq R_{T_2} \quad \Delta V_{T_B} = \left(R_{T_1} - R_{T_2}\right) I_B$$

$$\text{IF } R_{T_1} = R_{T_2} \quad \Delta V_{T_O} = R_T I_O$$

$$\Delta V_{T_C} = C\left(R_{T_1} - R_{T_2}\right) \frac{\Delta V}{\Delta T}$$

Figure 7.8. Simplified Equivalent Circuit of Dual Comparator with an Input Resistor Network

$R_T = 100\Omega \quad R_{T_1} = 95\Omega \quad R_{T_2} = 105\Omega$

$I_B = 25\mu A \quad I_O = .5\mu A \quad t_r = 10\text{nsec}$

ADJACENT LINE SIGNAL = 3V $\quad C = 2\text{pF}$

$\Delta V_{TB} = (10)(25)(10^{-6}) = \frac{1}{4}\text{ mV}$

$\Delta V_{TO} = (100)(.5)(10^{-6}) = \frac{1}{20}\text{ mV}$

$\Delta V_{TC} = (2)(10^{-12})(10)\left(\frac{3}{10^{-8}}\right) = 6\text{mV}$

Figure 7.9. An Example Showing Effect on Signal

**Reactive Coupling to Reduce Detection Errors** **(Figure 7.10)**

If the cause of these detection errors is the bias or offset current terms or the dc drift in these components, we can avoid them by using reactive coupling such as transformer or capacitive coupling as shown in this drawing. In general, with the video amplifier, the capacitive coupling would be required to isolate the comparator from the dc bias level in the output of the video amplifier. The capacitive coupling could be replaced by an inductor between the differential outputs to provide identical dc levels in the output and then feed these outputs to the dual differential comparator circuit discussed earlier. Both of these approaches offer the advantage of preamplification and removal of dc drift effects in increasing "0" and "1" noise margins for a given threshold detector. However, both suffer from a threshold that is frequency dependent.

Examples of integrated circuit sense amplifiers with a very narrow range of threshold voltage over a wide range of operating temperatures are the SN7520 series of sense amplifiers and the SN75236 sense amplifier whose design provides for a very stable and precise threshold in the comparator section. Further, these sense amplifiers offer a wide variety of output options including monostable multivibrator or flip-flop connections for pulse stretching or storage operations.

**Series 7520 Sense Amplifiers** **(Figure 7.11)**

In these devices, identical reference and input difference amplifiers are expected to exhibit the same temperature voltage and current changes so that the threshold remains relatively stable and independent of the "1" input voltage over a wide range of temperatures. The output of the basic comparator feeds a TTL gate configuration which provides a separate input for strobe control. In these devices the even numbers offer thresholds guaranteed to be within 4 millivolts of the reference voltage while the odd numbers offer a threshold within 7 millivolts of the reference. The SN55236 provides a threshold that remains within 2 millivolts of the reference voltage.

**Dual Channel Sense Amplifier for Detecting Signals on Two Bit Planes** **(Figure 7.12)**

These characteristics allow simple direct coupling to a wide variety of core types and sizes with a typical system configuration as shown using the SN7524 or SN7525 dual channel sense amplifier to detect the signals on two bit planes, each consisting of 4096 cores. The output of the amplifier then sets the appropriate bit flip-flop in the memory data register.

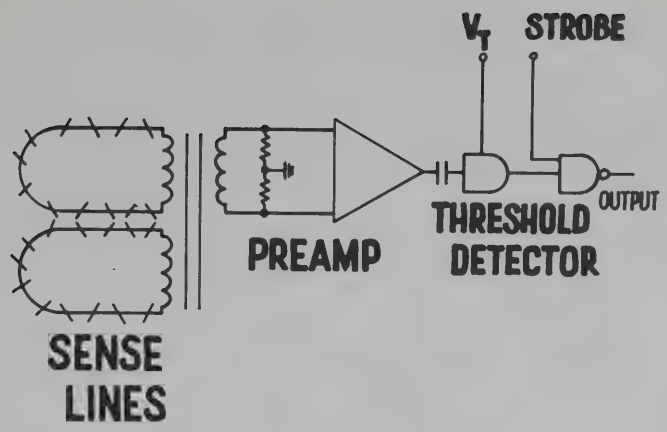



Figure 7.10. Reactive Coupling to Reduce Detection Errors

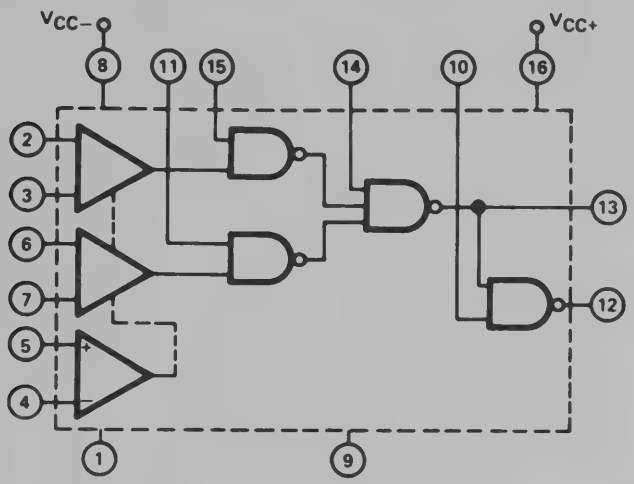



Figure 7.11. Series 7520 Sense Amplifiers

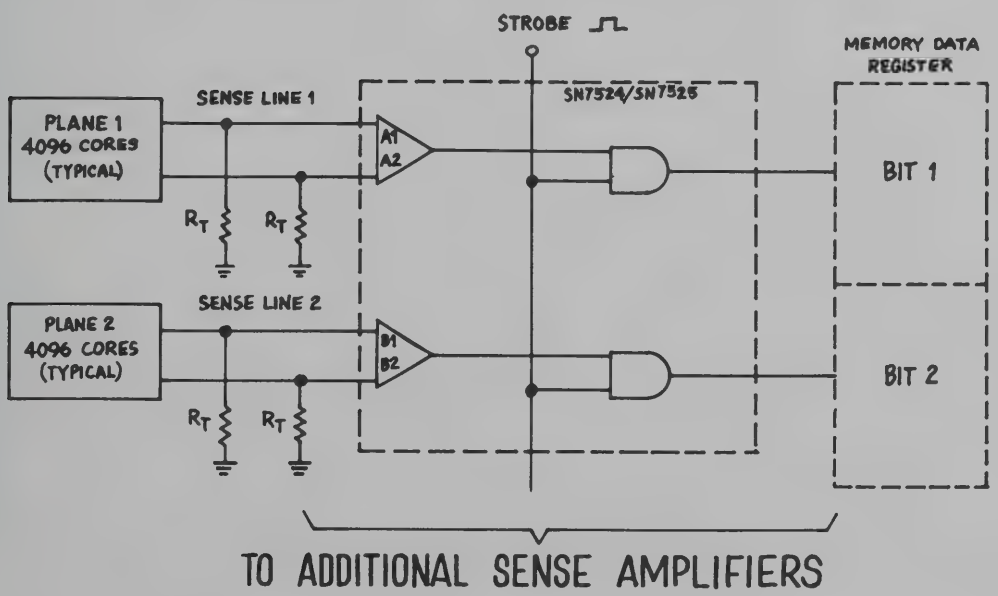



Figure 7.12. Dual Channel Sense Amplifier for Detecting Signals on Two Bit Planes

**SN7520 Connected to Provide Memory Data Storage Function** **(Figure 7.13)**

Other members of the SN7520 series offer more complex output capabilities. The SN7520 and SN7521 offer cascaded NAND gates which can be connected to provide the memory data storage function inside the sense amplifier circuit as shown.

**Alternative Connection of SN7520 for Memory Data Storage Function** **(Figure 7.14)**

An alternative connection is to use a monostable multivibrator connection of the type shown to meet pulse stretching requirements. The output pulse width would be proportional to R and C.

**Equation for Determining Output Pulse Width** **(Figure 7.15)**

The equation shown, used to determine output pulse width, is based on TTL logic thresholds of 1.3 volts and a logical "1" voltage level of 5 volts.

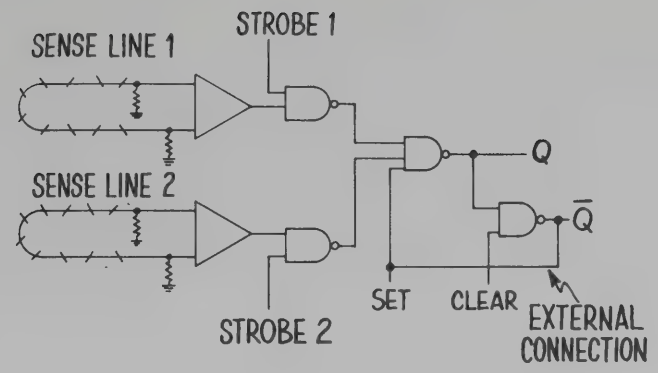



Figure 7.13. SN7520 Connected to Provide Memory Data Storage Function

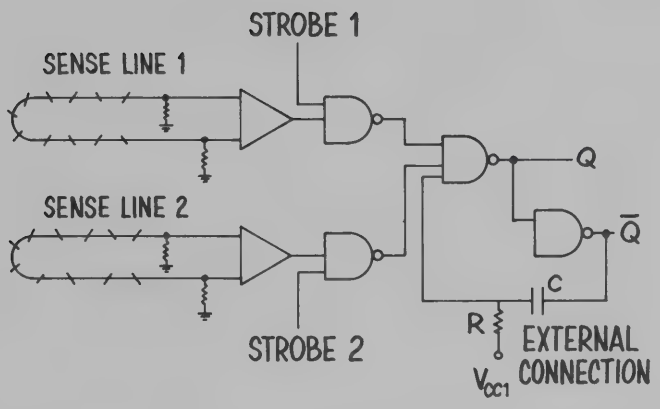



Figure 7.14. Alternative Connection of SN7520 for Memory Data Storage Function

$$T = RC \ln \frac{V_{CC_1} + V_{'1'}}{V_{CC_1} - V_{L.T.}} = RC \ln \frac{V_{CC_1} + 5}{V_{CC_1} - 1.3}$$

Figure 7.15. Equation for Determining Output Pulse Width

**SN7520 and SN7522 Connected to Sense a Large Number of Words** **(Figure 7.16)**

The SN7522 and SN7523 offer an open collector output for wired AND operation in conjunction with the SN7520 or SN7521 amplifiers. This is useful in cases where a large number of words are sensed as shown. In this case four sense lines allow sensing of a given bit of 4 times 4096 cores or 16,384 words with the SN7520 output wired to perform the memory data register function.

**Simple Comparator Connected as a Zero Crossing Detector** **(Figure 7.17)**

Before we conclude our discussion of sense amplifiers, we should examine some special sense detection problems which can readily be solved with the sense amplifier configuration. The first of these is the case where the "1" signal is a positive signal and the "0" signal is a negative signal. This situation can arise in certain types of memories such as bias or nondestructive read memories and the detection of certain magnetic tape magnetization storage patterns. In this case, a simple comparator can be used directly as shown to achieve reliable detection as a zero crossing detector.

**A Preamplifier Video Amplifier** **(Figure 7.18)**

Again, if the "0" positive and negative signals are of the order of the comparator offset voltage a preamplifier video amplifier may have to be used to provide acceptable noise margins. In this circuit, an SN72733 amplifier is used to provide the preamplification with an inductor connected between the outputs to remove any output dc offset in the video amplifier.

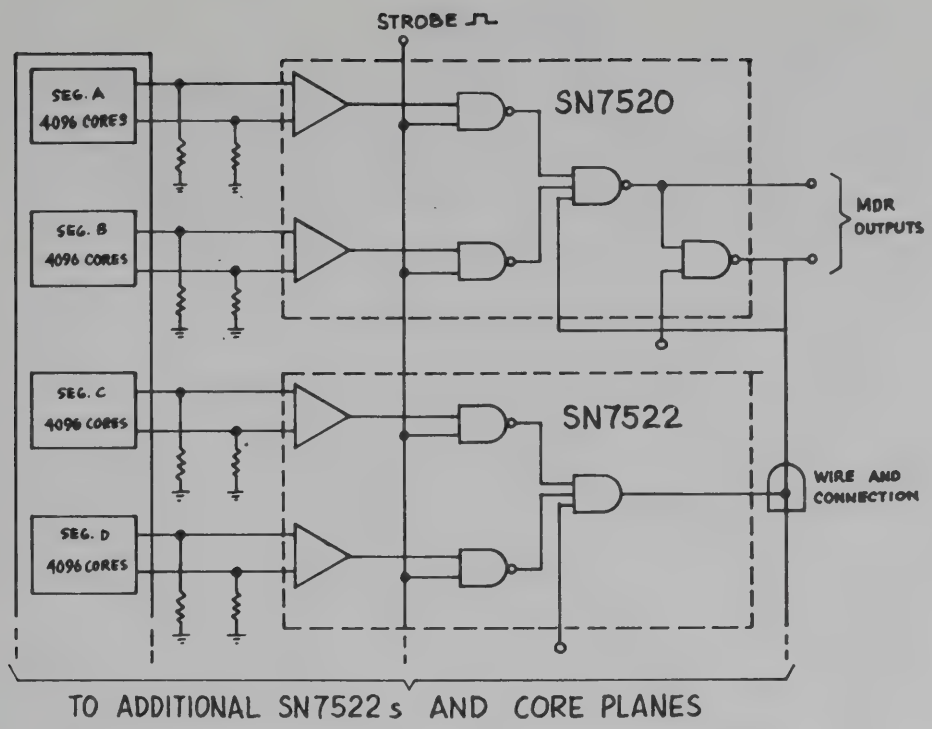



Figure 7.16. SN7520 and SN7522 Connected to Sense a Large Number of Words

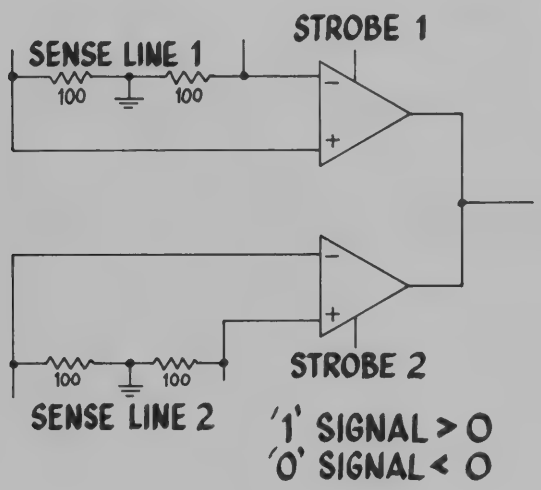



Figure 7.17. Simple Comparator Connected as a Zero Crossing Detector

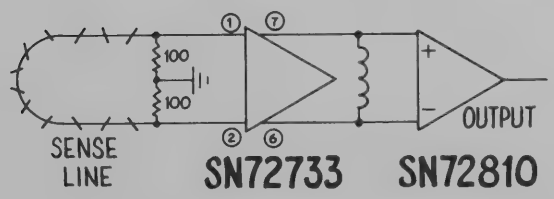



Figure 7.18. A Preamplifier Video Amplifier

**SN75108 Sense Amplifier Used in an MOS Application** **(Figure 7.19)**

For single polarity MOS signals you normally will choose sense amplifiers that have been designed specifically for use with such memories in these applications. Examples of such devices are the SN75208 sense amplifier with a ±10 millivolt threshold range and its lower performance cousin the SN75108 line receiver with a ±25 millivolt threshold range. An example application using the SN75108 is shown.

**Circuit to Strobe the Power Supplies to the Sense Amplifier** **(Figure 7.20)**

Another special application problem is the case where the standby power of the sense amplifier bank is too large because of excessive heat generation or power consumption. This can be avoided by strobing the power supplies to the sense amplifier so that they are only consuming power during their detection time period. A circuit for doing this is shown here. This circuit can drive the supply for several sense amplifiers. When the Q1 receives an input strobe pulse it turns on, causing the base emitter junction of Q2 to become strongly forward biased, saturating Q2. This causes the full supply voltage to be supplied to the sense amplifier, turning it on. When the strobe pulse is removed then Q1 turns off which turns Q2 off. This causes the supply voltage of the sense amplifier to fall to $V_{CC} - V_Z$ which can be adjusted to reduce the power consumption to any desired level. A similar circuit can be used to control the negative supply as well if needed.

## SUMMARY

We have discussed sense amplifiers primarily in terms of memory applications; however, these devices can be used to detect the presence of "0" and "1" signals in any digital data or telemetry system by proper choice of threshold voltages and strobe intervals. Because the core sense amplifier detects both positive and negative signals you do have to be careful in using this device as a general purpose threshold detector. However, since the sense amplifier does perform a double threshold detection it might be useful in certain A/D converter applications and limit detection circuits. Whatever the threshold detector applications, the sense amplifier can often be adopted to it and the core memory sense amplifier offers a data register or pulse stretching output to further enhance its applications possibilities.

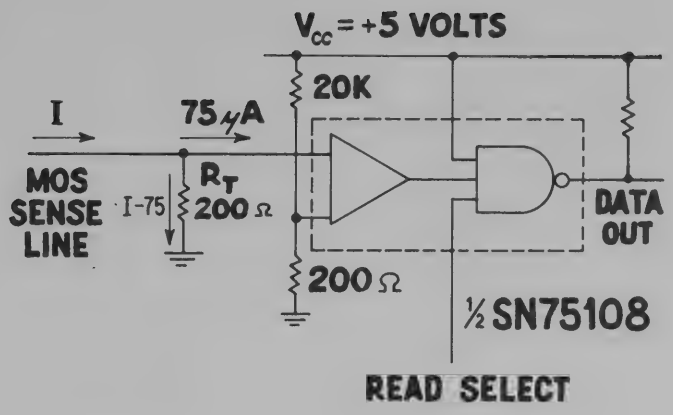



Figure 7.19. SN75108 Sense Amplifier Used in an MOS Application

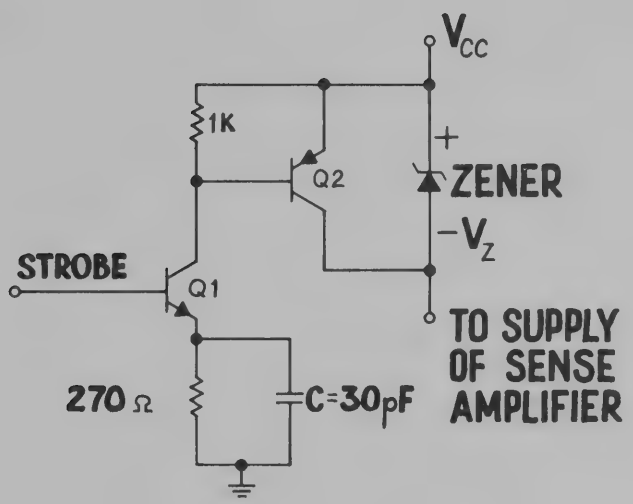



Figure 7.20. Circuit to Strobe the Power Supplies to the Sense Amplifier

# Lesson 8

# LINE DRIVERS AND RECEIVERS APPLICATIONS II — ADVANCED SYSTEMS

*The definition of the various data transmission systems and when and where they are used. Then a discussion of single-ended systems with available integrated circuits.*

# Lesson 8

# LINE DRIVERS AND RECEIVERS APPLICATIONS I — BASIC SYSTEMS

*This session is concerned with the operation and applications of line drivers and line receiver integrated circuits. These circuits are used for transmitting and receiving digital data along single wire, coaxial or twisted pair transmission lines.*

**Basic Single Line Transmission System** **(Figure 8.1)**

The transmission line is a single wire which may or may not be terminated in its characteristic impedance. The line driver applies either a constant voltage signal or a constant current signal to the line and the receiver is basically a threshold detector with a TTL compatible output that determines whether the received signal is a "0" or a "1."

**Equivalent Circuits of the Transmission System** **(Figure 8.2)**

A constant voltage mode driver is shown as a voltage source in series with the driver output impedance. In contrast, a constant current mode driver is shown as a current source in parallel with the driver output impedance. The line is represented as a single resistor computed by multiplying the line resistance/foot times the line length. The receiver is replaced by its input resistance and the input voltage at the receiver is computed for both types of circuits, representing both types of drivers. Thus, the effect of line attenuation or voltage drop is easily determined.

**Effects of Noise on Data Transmission** **(Figure 8.3)**

If a threshold detector type of receiver with an adjustable threshold is used, the output is a "1" when the signal is above the threshold voltage, and is a "0" when the signal is below the threshold voltage. The threshold is placed halfway between the expected "0" and "1" signal levels to achieve maximum and equal "0" and "1" level noise margins. If there is too much noise an error results in the receiver output. To achieve error-free transmission in a single wire line, a receiver signal voltage must be provided that is at least twice as large as the noise signal.

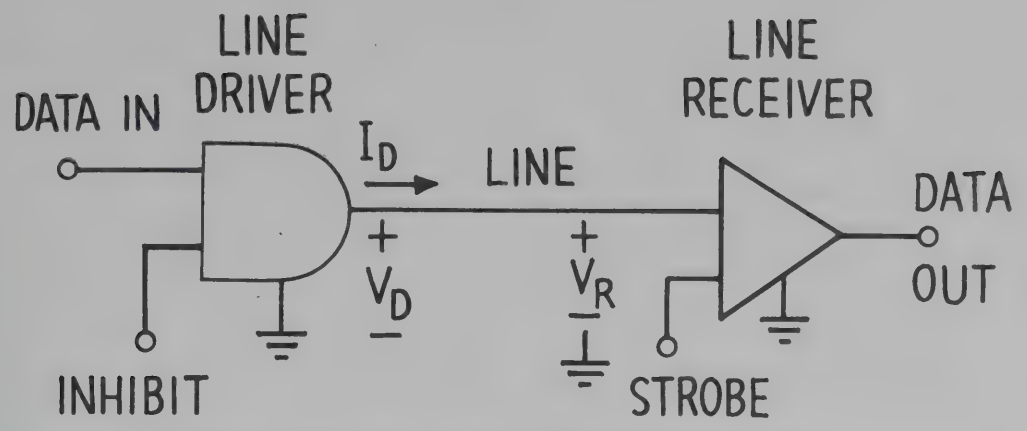
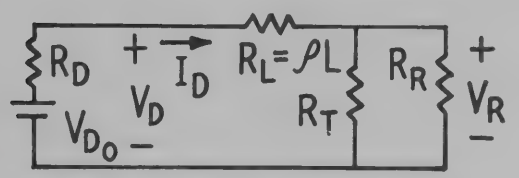
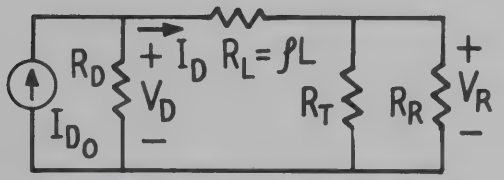



Figure 8.1. Basic Single Line Transmission System




CONSTANT VOLTAGE DRIVER

$$V_R = \frac{\left(\frac{R_R R_T}{R_R + R_T}\right) V_{D_O}}{R_D + R_L + \frac{R_R R_T}{R_R + R_T}}$$




CONSTANT CURRENT DRIVER

$$V_R = \frac{\left(\frac{R_R R_T}{R_R + R_T}\right) I_{D_O} R_D}{R_D + R_L + \frac{R_R R_T}{R_R + R_T}}$$

Figure 8.2. Equivalent Circuits of the Transmission System

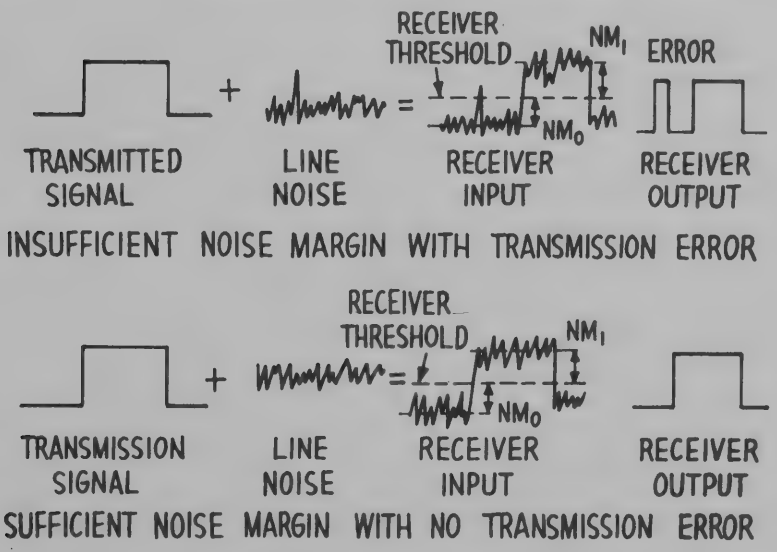



Figure 8.3. Effects of Noise on Data Transmission

**Effect of Hysteresis on Noise Margins** **(Figure 8.4)**

Another way to increase the receiver noise margin uses a receiver with a variable hysteresis. The hysteresis is the difference between the threshold levels required to switch from a "0" to "1" output which is $V_{T+}$ and that required to switch from a "1" to a "0" output level which is $V_{T-}$. The "0" noise margin is the difference between $V_{T+}$ and the "0" input voltage level, and the "1" noise margin is the difference between the "1" input voltage level and $V_{T-}$. By increasing the separation between $V_{T+}$ and $V_{T-}$, that is, increasing the hysteresis, both the "0" and "1" noise margins can be increased considerably. Of course, the hysteresis does decrease the receiver sensitivity.

**Effect of Ground Shift on Data Transmission** **(Figure 8.5)**

There are other effects that can drop the transmission reliability or noise margins by reducing the difference between the "0" and "1" voltage levels. One of these effects, the ground shift problem, occurs when the grounds at the receiver and transmitter stations are not the same. This causes the relative threshold at the receiver to offer poor noise margin for one signal level or another. This problem would generally be improved by a shielded cable, or, in the case of a single room facility, having a common ground wire linking all equipment.

**Single-Ended Transmission System Components Requirements** **(Figure 8.6)**

Figure 8.6 summarizes the properties required of transmission system components for single-ended transmission.

**Basic Constant Voltage Mode Driver** **(Figure 8.7)**

The input portion of the driver consists of a TTL input gate with inputs provided for data and inhibit inputs; a level translator uses zener diodes in series with the signal path; and a totem-pole output increases the current capability with a Darlington output configuration.

**Basic Constant Current Mode Driver** **(Figure 8.8)**

This driver has the same type of input and level translational circuitry as the constant voltage mode driver; it has a differential-amplifier, constant-current, and source-switch output. Also, this type of driver must have a single-ended to differential-ended converter, which is a differential amplifier with a single input.

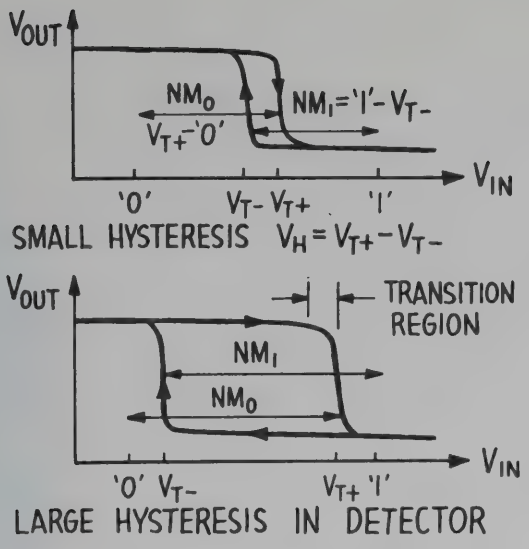



**Figure 8.4. Effect of Hysteresis on Noise Margins**

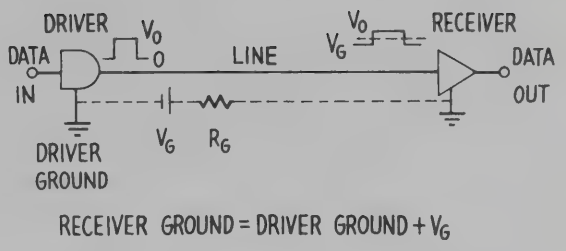



**Figure 8.5. Effect of Ground Shift on Data Transmission**

| LINE | CONSTANT CURRENT DRIVERS | CONSTANT VOLTAGE DRIVERS | RECEIVERS (SINGLE-ENDED AND DIFFERENTIAL) |
|---|---|---|---|
| LOW RESISTANCE SHIELDED IF NOISY ENVIRONMENT | HIGH OUTPUT CURRENT HIGH OUTPUT POWER HIGH OUTPUT IMPEDANCE | HIGH OUTPUT VOLTAGE HIGH OUTPUT POWER LOW OUTPUT IMPEDANCE | HIGH SENSITIVITY HIGH INPUT IMPEDANCE ADJUSTABLE HYSTERESIS ADJUSTABLE THRESHOLD |

**Figure 8.6. Single-Ended Transmission System Components Requirements**

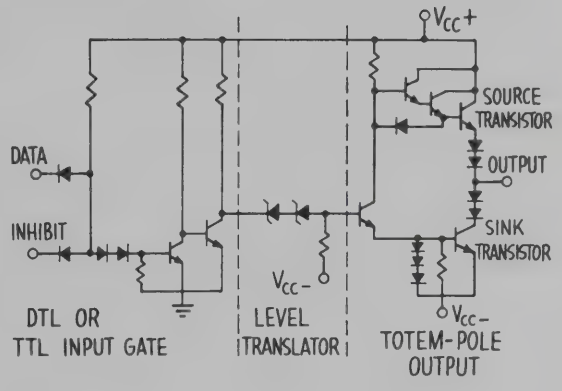



**Figure 8.7. Basic Constant Voltage Mode Driver**

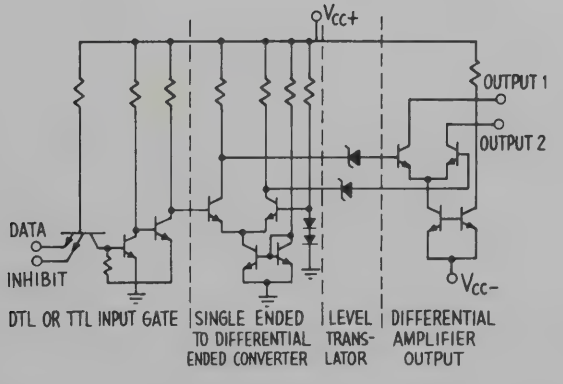



**Figure 8.8. Basic Constant Current Mode Driver**

**Hysteresis and Threshold Control Circuitry** **(Figure 8.9)**

The basic single-ended line receiver is a threshold detector with controlled positive feedback used to provide the threshold and hysteresis control. The amount of current available for feedback is controlled by the collector connection of the feedback transistor. To achieve a maximum hysteresis terminal T would be connected to the $V_{CC1}$ terminal. For minimum hysteresis, the T terminal is left unconnected.

The rest of this session is concerned with special applications problems and their solutions beginning with telephone-line data transmission. The opportunity for remote control and data processing using existing communications networks, is limited only by the ability to transmit the data between a digital device and a telephone MODEM. Modem is short for modulator-demodulator.

**Use of Standard Commercial Line** **(Figure 8.10)**

The basic data transmission configuration for the use of existing communications networks is illustrated in Figure 8.10. Shown are the data terminal equipment, its associated driver and receiver, the line connection to the modem and its associated receiver and driver. The modem interfaces to a standard telephone line.

**Comparison of EIA and MIL Standard Conditions** **(Figure 8.11)**

Shown are the basic requirements of interfacing between a digital transmission line and a commercial or military modem. Both requirements allow no line terminations other than the line receiver input impedance. The receiver input impedance should be 3K to 7K for EIA applications and greater than 6K for MIL standard. Similarly, the MIL standard allows a maximum of ±6 volt line voltage while the EIA allows the full supply range.

**EIA and MIL Standard Driver Configurations** **(Figure 8.12)**

Generally, the same circuits can be used to satisfy both standards by using proper external components and terminal connections. The only real difference in the connection diagrams is the incorporation of back-to-back 5.2 volt zener diodes on the output to meet the voltage limit specification of MIL-STD-188.

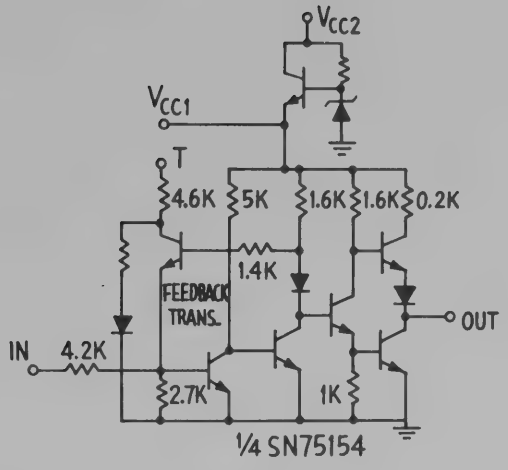



Figure 8.9. Hysteresis and Threshold Control Circuitry

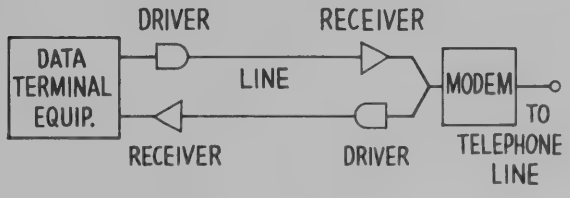



Figure 8.10. Use of Standard Commercial Line

| | EIA-RS 232C | MIL-STD-188 |
|---|---|---|
| LINE SIGNAL LIMITS | ±5 TO ±15 | ±6 |
| RECEIVER INPUT IMPEDANCE | 3K Ω TO 7K Ω | ≥ 6K Ω |
| HYSTERESIS | | $V_T$ ± 0.6 VOLTS |

Figure 8.11. Comparison of EIA and MIL Standard Conditions

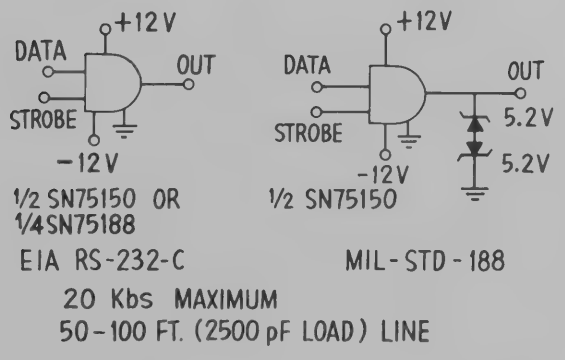



Figure 8.12. EIA and MIL Standard Driver Configurations

**EIA and MIL Standard Receiver Connections** **(Figure 8.13)**

The line receivers can generally be used in either application if the correct hysteresis and input impedance control connections are used as specified by the circuit manufacturer. For example, with the SN75152 receivers, the MIL standard hysteresis and input impedance can be achieved by simply leaving the hysteresis control and the $R_T$ terminal open. The EIA conditions are produced by connecting the hysteresis control to $V_{CC-}$ and the $R_T$ to ground.

With general purpose transmission problems, dual supply circuits or single supply circuits may be used. Many designers prefer the simple single supply configuration unless the dual power supplies are already available in the system.

In addition to the EIA and MIL standards, an important interface standard is required by IBM for all data transmission into or out of a piece of IBM equipment. Several manufacturers make circuits that meet these specifications. For example, SN75123 and SN75124 line circuits meet these requirements with single 5-volt supply operation by using a circuit of the type shown in Figure 8.14.

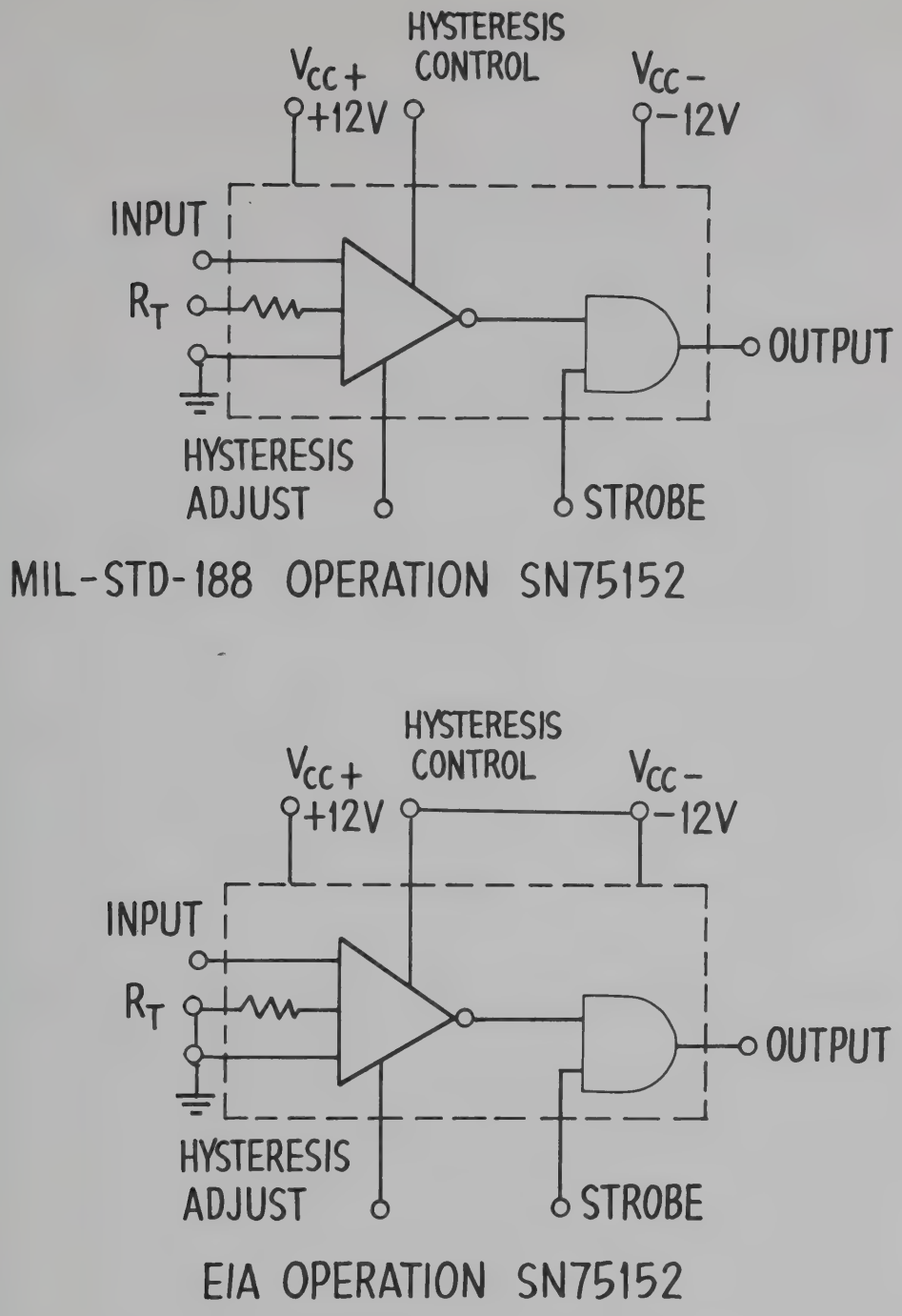



**Figure 8.13. EIA and MIL Standard Receiver Connections**

**IBM Interface Configuration** **(Figure 8.14)**

The IBM specifications require 96-Ω line terminations which improve the line noise and reflection performance but increase the driver power requirements. IBM drivers must provide 59 mA at 3.11 volts. Thus the IBM standard circuits have a common collector output which connects to the 96-Ω termination. The IBM specification also requires a receiver that has a switching threshold between 0.7 and 1.7 volts so that a low hysteresis is allowed but not required. In addition, the receiver circuit must withstand a 7-volt input with power on and a +6 volt or −0.15 volt input with the power off.

Now that the solutions to standard specifications data transmission problems have been examined, special transmission problems are considered. Such problems include medium speed transmission rates over relatively short lines.

In these special cases, a wide range of line impedances along with their proper terminations is allowed. Coaxial lines offer the best noise immunity. Their disadvantage is that they exhibit a higher capacitance load on the driver than would be the case with a twisted pair or single wire line.

Intermediate in all respects between single wire and coaxial lines is the twisted pair line when used in single ended transmission systems. It offers limited shielding properties in single ended applications but offsets this with an increase in capacitive loading over that of the single wire line. Measuring the line impedance and providing the proper termination may be worthwhile in situations where reflections are dropping the transmission reliability to a marginal level. In general, where termination impedances are employed, it is advisable to use terminations on both ends of the lines.

There are four basic driver-line-receiver configurations that can be used effectively for special purpose data transmission. Three of them have already been discussed. The first is the non-terminated EIA/MIL standard configuration. The second is the configuration with the line terminated in its characteristic impedance at either or both ends. The third is the IBM standard with common collector output and both ends of the line terminated in its characteristic impedance.

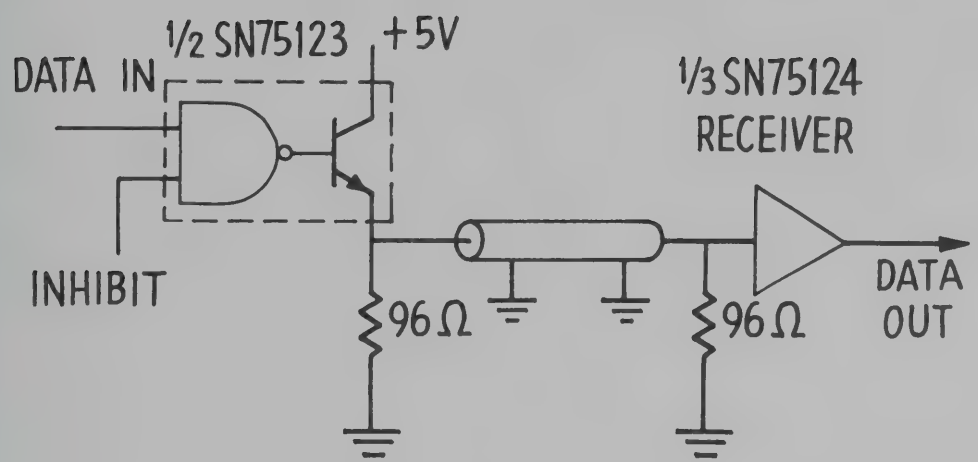



**Figure 8.14. IBM Interface Configuration**

**Active Pull-Up Transmission Line Termination** **(Figure 8.15)**

A fourth method that has not been discussed is shown in Figure 8.15. The line is terminated at both ends and has a common emitter driver output with the termination resistors providing active pull-up. This configuration is used with circuits that have grounded emitter outputs with an open collector as an output terminal, such as the SN75450 series of peripheral drivers. In addition, current mode drivers could be used in these configurations to obtain improved system performance in terms of data rates, line length, or noise immunity for a given driver power output.

There is also considerable freedom in receiver selection, though generally most manufacturers provide receivers that are compatible with a given driver, and such a receiver would normally be the most logical choice for that particular driver.

**Use of Differential Receiver in Single-Ended Transmission Line** **(Figure 8.16)**

Shown is an application of the differential drivers and receivers to a single line system. The differential input comparator of the receiver allows direct adjustments of the switching threshold and there is no hysteresis. Other receivers with lower sensitivity could be used. For example, the SN75182 and SN75115 have threshold sensitivities of ±0.5 volt. However, this does not produce as significant a gain in noise immunity from lower sensitive thresholds.

**Use of Differential Comparator as Receiver** **(Figure 8.17)**

A line receiver can be realized by using a comparator-TTL gate arrangement. Such an arrangement is shown in Figure 8.17. It is also possible to use a sense amplifier. Differential comparator type circuits have the same limitations of the differential line receiver in single-ended applications.

**20 MHz Transmitter** **(Figure 8.18)**

In all of the special system configurations discussed thus far, it is possible to achieve high performance on either the line length or the data rate even with single line systems. Shown in Figure 8.18 is an example of a high data rate short line system. Advantage is taken of the excellent characteristics of the SN75451 peripheral driver and the use of coaxial line of 100 foot length to achieve a 20 MHz bit rate.

**Single-Ended Transmission Frequency to 0.5 MHz** **(Figure 8.19)**

Similarly the SN75450 peripheral driver can be used to achieve a lower bit rate of 0.5 MHz over a line of 1000 foot length as shown in Figure 8.19.

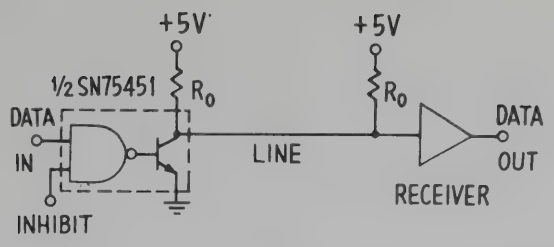



Figure 8.15. Active Pull-Up Transmission Line Termination

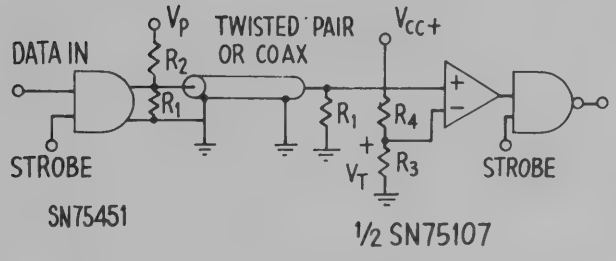



Figure 8.16. Use of Differential Receiver in Single-Ended Transmission Line

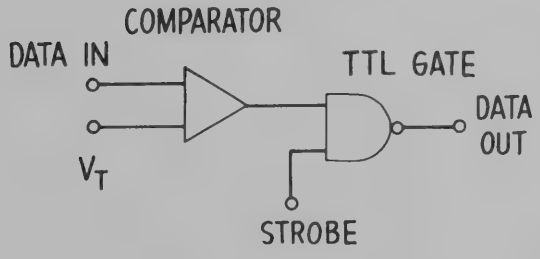



Figure 8.17. Use of Differential Comparator as Receiver

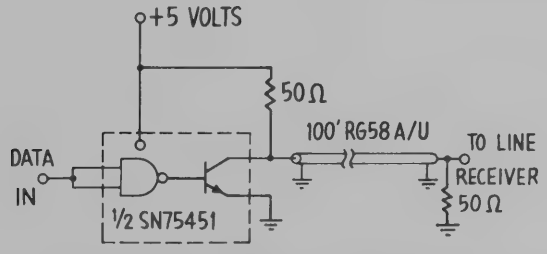



Figure 8.18. 20 MHz Transmitter

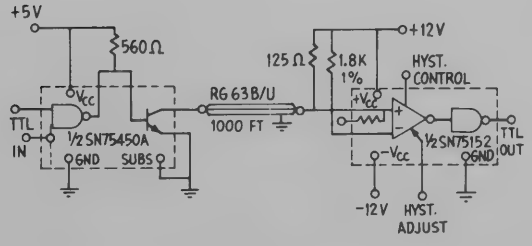



Figure 8.19. Single-Ended Transmission Frequency to 0.5 MHz

**Party Line Data System** **(Figure 8.20)**

An extension of the special purpose transmission problem is the case where there are more than two data stations. This type of system is called a party line or half duplex system. In such systems a driver can be transmitting data to one or more receivers at various destinations. Similarly, provision is made for two-way communication. This type of operation complicates the transmission problem in two ways. First, the line must be terminated at both ends to avoid all reflection problems. Secondly, the source and destination pair must be uniquely determined, i.e., only one driver can be active at any given time, and further, often only one receiver can be active. The simplest solution to these problems is to have a line busy detector and indicator at each terminal, much as is used in an office intercommunication system, and a driver would access the line only when the line is free.

For those systems that have a large number of receivers and drivers in them, it becomes very important that the receivers have high input impedance and that all inactive drivers have high output impedances. Otherwise considerable signal loss can occur with a corresponding undesirable increase in driver power requirements. To remedy this problem, some three-state drivers are manufactured that exhibit the standard TTL emitter follower source in the "1" state, the common emitter sink in the "0" state, and a high output impedance or open transistors in the inhibit or inactive state.

## SUMMARY

The basic data transmission problem has been defined and the various solutions to that problem have been examined. Discussion has concentrated on the simpler single-ended data transmission system with its short path length or low bit applications. Such single-ended systems will cover most general purpose data transmission problems. These concepts are extended in other sessions to the differential line system with its application to high bit range, long line systems, covering both single party and party line applications.

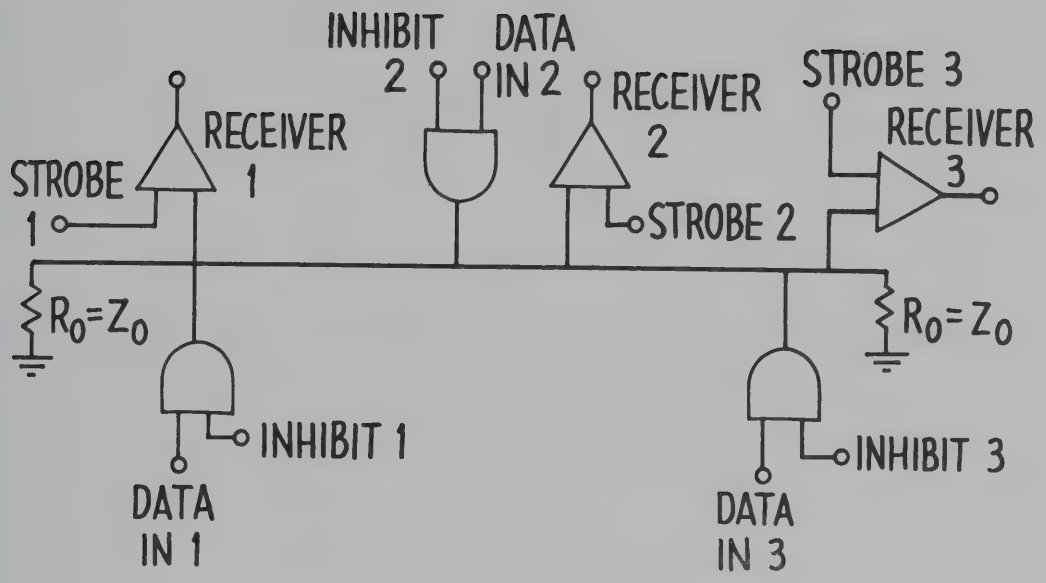



Figure 8.20. Party Line Data System

# Lesson 9

# LINE DRIVERS AND RECEIVERS APPLICATIONS II — ADVANCED SYSTEMS

*Applications examples continue with differential and party-line systems discussed and the advantages and disadvantages of using particular integrated circuits.*

# Lesson 9

# LINE DRIVERS AND RECEIVERS APPLICATIONS II — ADVANCED SYSTEMS

*This discussion of line drivers and receivers will cover the more advanced systems involving high data rate transmissions or long path length systems in noise environments. The transmission line will be dual lines, and the line circuits will have differential amplifier configurations.*

**Effect of Noise on Dual Line Transmission Systems** **(Figure 9.1)**

Environmental disturbances do affect the transmitted signal as shown in this drawing. While disturbances cannot be avoided, especially with long line systems, much of the effects of these disturbances on the signal can be eliminated by using either twisted pair lines or balanced dual connector coax lines, and then detecting the signal with sensitive differential comparator receivers having high common mode rejection. Such a system can reliably send and receive data even under conditions of severe signal attenuation and in the presence of severe environmental noise.

**Detection of Signals in Presence of High Common Mode Noise** **(Figure 9.2)**

As an example of the improvements that can be expected in these differential systems, the typical common mode voltages of ±3 volts can be tolerated without affecting the differential detection sensitivity of from 10 to 25 millivolts, and allowed noise voltage of up to 100 times the signal voltage, without preventing reliable signal discrimination. A typical response is shown here where a clear, reliable output signal is obtained even though considerable common mode noise is present. The conditions of this test are a 50 mV peak-to-peak 10 kHz input signal in the presence of 4 volts peak-to-peak noise using the SN75108 line receiver.

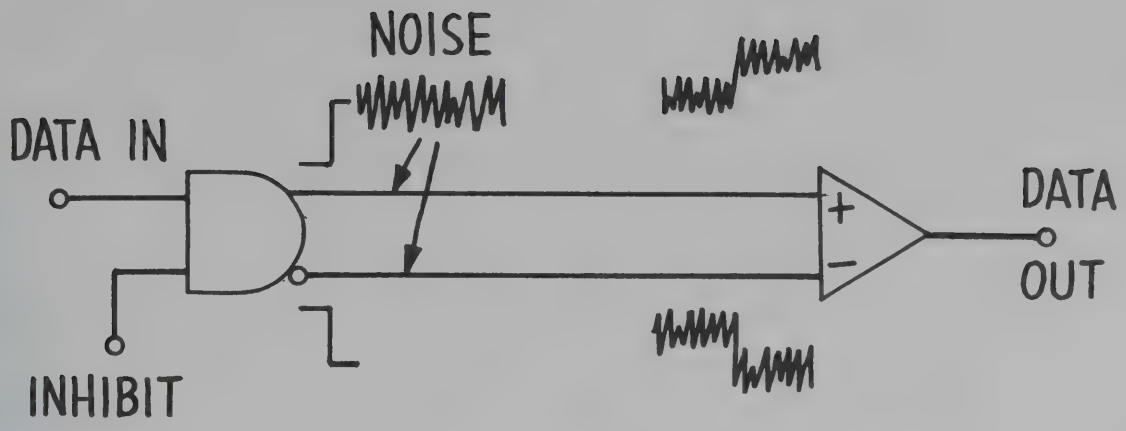



Figure 9.1. Effect of Noise on Dual Line Transmission Systems

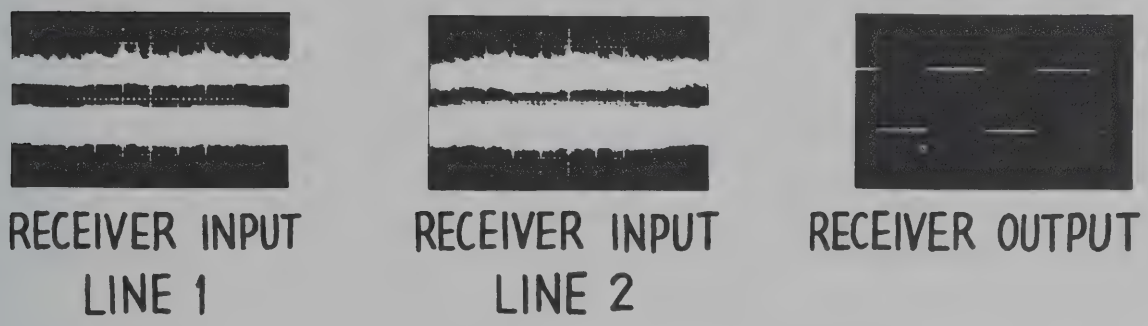



Figure 9.2. Detection of Signals in Presence of High Common Mode Noise

**Receiver Threshold Placement** **(Figure 9.3)**

If the noise has a differential component, the situation must be handled by providing an input signal that is larger than the differential mode noise, and by discriminating between signal and noise by proper choice of the receiver threshold. An example of this technique is illustrated in this drawing.

In order to be able to intelligently design a high performance data transmission system, look into the driver, receiver and line performance parameters carefully. Choice of the transmission line media has considerable effect on the noise characteristics of the transmission. In the types of systems considered in this lesson, it is important to always terminate both ends of the line with its characteristic impedance to avoid signal reflections and noise spikes. The coaxial lines have advantages in this respect. The disadvantage of the coaxial line is its weight, cost, and high capacitance to ground. A simple twisted pair line offers the advantage of low cost and weight, and small parasitic capacitance to ground, and such a line exhibits low differential mode noise components.

**Measurement of Line Impedance** **(Figure 9.4)**

The main disadvantage of the twisted pair is the possibility that the line impedance may have to be determined experimentally. Such measurements are easily made with an R-X meter as outlined here. The characteristic impedance of the line is the geometric mean of the open circuit and short circuited impedances.

**Characteristic Impedances of Parallel Wire and Coaxial Transmission Lines** **(Figure 9.5)**

This figure compares the types of impedances obtained with parallel wire and coaxial wire dual line systems. This illustration shows the variation of the line impedance with the dimension ratio of the particular line geometry. The dimension ratio is defined to be the ratio of wire spacing to wire diameter for parallel wires, and the ratio of the inner diameter of the shield to the inner wire diameter for the coaxial line.

**Equivalent Circuit for Differential Line with Constant Current Driver** **(Figure 9.6)**

The length of line that can be used for reliable signal transmission depends on the signal attenuation per foot, the receiver sensitivity, and the driver output signal. The line signal attenuation depends primarily on the line resistance per foot and the line capacitance per foot. The attenuation depending on the line resistance is primarily an ohmic drop. This equivalent circuit can be used to compute the attentuation.

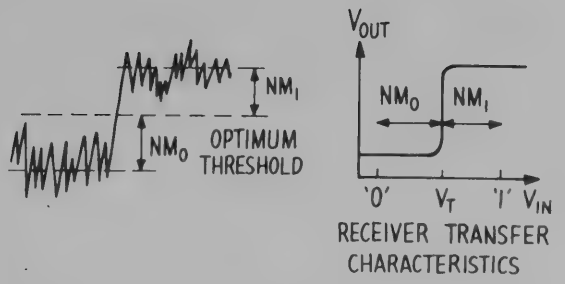



Figure 9.3. Receiver Threshold Placement

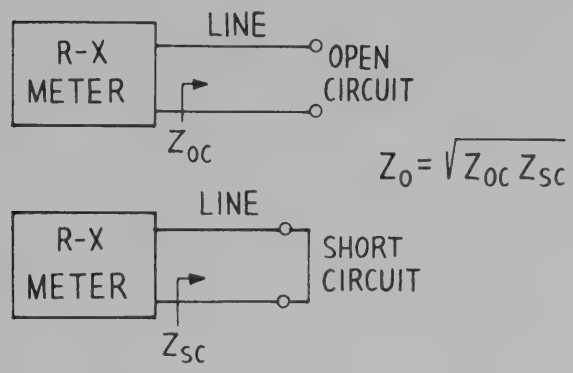



Figure 9.4. Measurement of Line Impedance

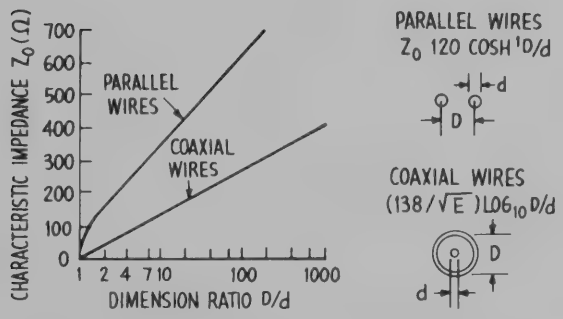



Figure 9.5. Characteristic Impedances of Parallel Wire and Coaxial Transmission Lines

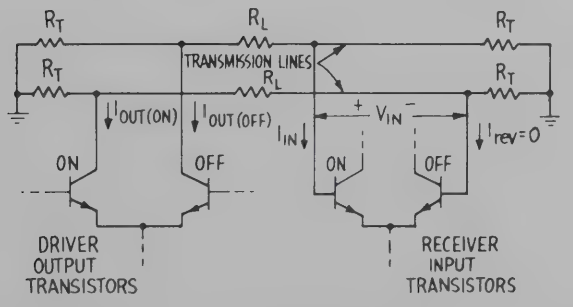



Figure 9.6. Equivalent Circuit for Differential Line with Constant Current Driver

**Equations for Computing Attenuation** **(Figure 9.7)**

In this computation, the effects of the driver currents $I_{OUT(on)}$ and $I_{OUT(off)}$ and input current producing a voltage $V_{in}$ have been combined by superposition to yield Equation (1). By solving this relationship for the zero line length case as is shown in Equation (2), the line length allowed can be predicted for a given driver input, line resistivity, and the receiver sensitivity as shown in Equation (3).

**Resistive Attenuation with Length of Typical Transmission Lines** **(Figure 9.8)**

This figure shows the receiver input voltage versus line length. For a receiver sensitivity of 25 millivolts, the line length possible for either a 0.01 Ω/foot line or a 0.05 Ω/foot line is shown to be 75,000 and 10,000 feet respectively. Line resistivity has a far greater effect on the theoretical line length than receiver sensitivity. Increasing the receiver sensitivity by 2 1/2 times to 10 millivolts increases the line length of a 0.05 Ω/foot line from 10,000 feet to about 15,000 feet, while decreasing the resistivity by a factor of 2 1/2 times increases the theoretical line length to over 20,000 feet. This is a theoretical limit and other effects have to be considered to completely estimate the allowed line length for a given situation. One of these effects is the other attenuation effect, the capacitive loading of the line.

**Capacitance per Foot of Transmission Line** **(Figure 9.9)**

The capacitance of the line will also limit the length of the line obtainable with a given driver at a given bit rate with a given receiver sensitivity. The capacitance per foot in picofarads/foot for the two types of lines is given as proportional to the line dielectric constant over the log of the dimension ratios. These relationships indicate that the coaxial line has twice the capacitance per foot of the twisted pair.

**Capacitive Effects on Transmission Line** **(Figure 9.10)**

This shows the equivalent circuit for 100 feet of line, with the relationship for output voltage in terms of the input voltage derived from a simple voltage divider relationship. The higher the capacitance or the frequency, the lower $V_{OUT}$ and the lower the allowed line length, since the attenuation is higher.

**Experimental Attenuation Curves** **(Figure 9.11)**

Normally experimentally determined attenuation curves of the type shown here are used where the attenuation in decibels per 100 feet is plotted versus frequency for coaxial and twisted pair lines. A longer line length is obtainable with the coaxial line than with the twisted pair line.

1) $V(L) = V_{IN_R} = \frac{R_T}{Z_{RT}+R_L}\left[(I_{OUT(ON)} - I_{OUT(OFF)} - I_{IN}) - R_L I_{IN}\right]$

2) $V(L) \approx \frac{V(0)}{1+\frac{R_L}{2R_T}}$ IF $R_L \ll 2R_T$

$V(0)$ = RECEIVER INPUT FOR ZERO LINE LENGTH
IF $V(L) = V_R$ = RECEIVER SENSITIVITY

3) $L_t = \frac{2R_T}{\rho}\left(\frac{V(0)}{V_R} - 1\right) = \frac{R_0}{\rho}\left(\frac{V(0)}{V_R} - 1\right)$

Figure 9.7. Equations for Computing Attenuation

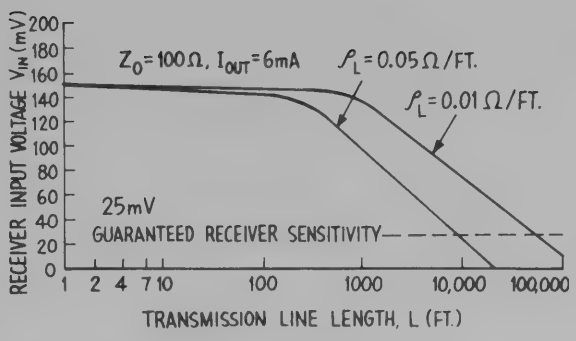



Figure 9.8. Resistive Attenuation with Length of Typical Transmission Lines

TWO WIRE LINE

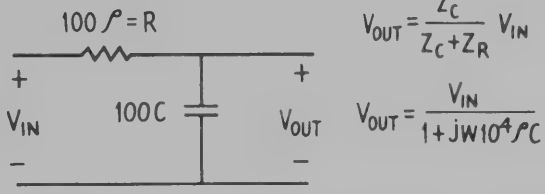
$C = \frac{3.68\,\epsilon r}{\log d/a}$ pF/FT.


a = RADIUS OF WIRE

COAXIAL LINE

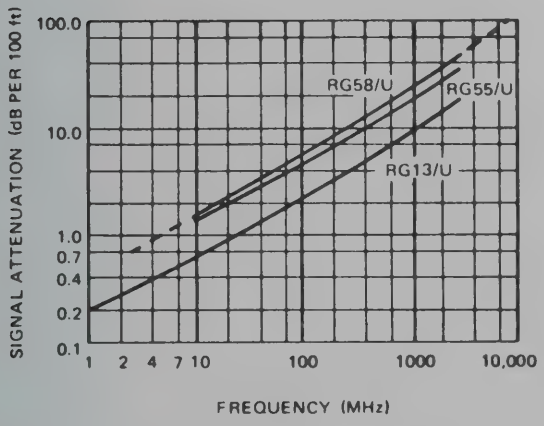
$C = \frac{7.35\,\epsilon r}{\log b/a}$ pF/FT.


Figure 9.9. Capacitance per Foot of Transmission Line

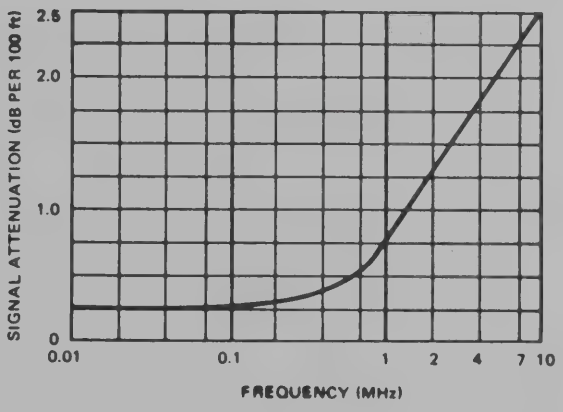



EQUIVALENT CIRCUIT OF 100 FEET OF LINE

Figure 9.10. Capacitive Effects on Transmission Line




*Attenuation With Signal Frequency in Typical Coaxial Cables*




*Signal Attenuation With Frequency in Twisted-Pair Transmission Line (AWG 22 Solid Wire With 0.060-in Plastic Cover, Twisted 4.5 Times Per Foot)*

Figure 9.11. Experimental Attenuation Curves

**Theoretical Line Length Relationships** **(Figure 9.12)**

The line length that would be allowed for a given reciever sensitivity, frequency of operation, and driver output can be computed from the relationship given here.

**Example Line Length Computations** **(Figure 9.13)**

For a sample computation of line lengths, notice this figure. In this example situation, the capacitive attenuation would be the limiting factor. This theoretical length would then be the first step in designing the transmission line configuration for a given data rate and line length.

To further characterize and predict the line and system performance, consider the line transit time and transient effects. The signal velocity on most coaxial lines is about 65% the speed of light, which would result in a typical propagation delay for such a line of 1.5 ns/foot of line. This would result in delays in the microsecond range on a 1000-foot line. This would effect the minimum time between transmissions on a two-way or party-line system. Transient line effects such as ringing or overshoot are not as severe a problem with long terminated transmission lines as they are in short line connections between fast rise time gates on printed circuit boards or in board-board cable connections.

**One-Way Transmission** **(Figure 9.14)**

This is one of several configurations used to achieve proper termination. In all cases the termination is to ac ground (which could be a positive or negative or ground dc voltage supply with 0 ac impedance). This is the simplest termination where only one line is terminated in a single ended system. In this case $R_T = R_O$.

**Party-Line Single-Ended Transmission** **(Figure 9.15)**

In the next most complex single-ended system, both ends of the active lines are terminated and $R_T$ would still equal $R_O$, the characteristic impedance of the line.

**Differential Transmission Single Termination** **(Figure 9.16)**

The simplest differential circuit is shown here. This circuit also has $R_T = R_O$.

$$L_{t_\rho} = \frac{R_0}{\rho}\left(\frac{V(0)}{V_R} - 1\right) \qquad L_{t_c} = \frac{2000}{A} \text{ LOG } \frac{V(0)}{V_R}$$

$\rho$ = LINE RESISTANCE/FOOT

$R_0$ = LINE CHARACTERISTIC RESISTANCE

A = ATTENUATION IN db/100 FEET

LINE RESISTANCE LIMITATION

LINE CAPACITANCE LIMITATION

**Figure 9.12. Theoretical Line Length Relationships**

RG 14 A/U COAXIAL CABLE

$R_0 = 52 \quad \rho = 0.01 \quad A = 0.44$ db/100 ft $\quad f = 15$ MHz

$V_R = 25$ mV $\qquad V(0) = 75\text{mV} \approx \left(\frac{R_0}{4}\right) I_{OUT(ON)}$

$$L_{t_\rho} = \frac{52}{0.01}\left(\frac{75}{25} - 1\right) = 10{,}400 \text{ FEET}$$

$$L_{tc} = \frac{2000}{0.44} \text{ LOG } \frac{75}{25} = 2{,}180 \text{ FEET}$$

**Figure 9.13. Example Line Length Computations**

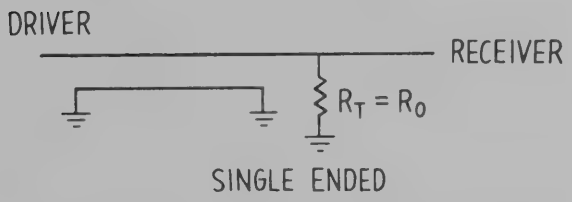



**Figure 9.14. One-Way Transmission**

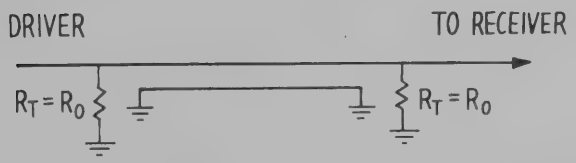



**Figure 9.15. Party-Line Single-Ended Transmission**

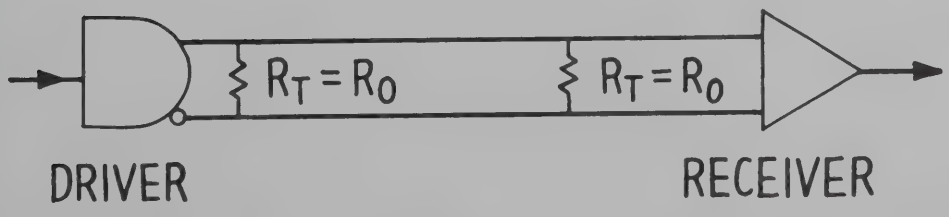



**Figure 9.16. Differential Transmission Single Termination**

**Differential Transmission Dual Termination** **(Figure 9.17)**

In the most complicated case, the $R_T$ is 1/2 $R_o$.

Much of what has been discussed thus far regarding line characteristics applies equally well to single-ended or differential data transmission. The primary difference in the two systems is in the detection process at the receiver. In a long line system, the important receiver parameter is its sensitivity, and any hysteresis tends to reduce this sensitivity, so that for long line transmission for reasonable driver voltages and currents it is more reasonable to use the differential comparator type of receiver with high sensitivity and low hysteresis. The dual differential line configuration depends on receiver common mode rejection and low differential noise signals to achieve noise immunity. Even a single-ended long line system would still require high receiver sensitivity and again tend to use a no-hysteresis differential receiver. In order to achieve high bit rate operation, the receiver must have a fast response time, since the receiver must have completely detected the previous bit before it can operate on the bit presently being sent.

**Summary of Receiver Properties** **(Figure 9.18)**

The properties of various typical line receivers intended for single-ended line and differential line applications are summarized in this table.

**Input Attenuators to Increase Receiver Common Mode Limit** **(Figure 9.19)**

For those cases where a large common mode voltage is expected, trade receiver sensitivity for the common mode voltage limit by using simple voltage divider attenuators is shown in this drawing. In this case a common mode signal of up to ±15 volts can be applied to the SN75107. The receiver sensitivity would in turn be degraded to a ±125 millivolt level.

In general, since long line data rates tend to be practically limited to 10 to 20 MHz, which would require 50 nsec or less cycle time, the receiver sensitivity may be a more important parameter than receiver response time, as most receivers offer response times of less than 50 nanoseconds. In addition the use of single supply operation may eliminate the feasibility of using most comparator or sense amplifier realizations and force the use of one of the conventional single supply line circuits whose sensitivity is limited to about 0.5 volt.

**Typical Driver Characteristics** **(Figure 9.20)**

As was the case in line receivers, the driver characteristics required may be in another type of driver such as a peripheral driver. Here is a summary of typical driver characteristics. Most drivers have fast switching times of less than 30 nanoseconds and both single supply and dual supply drivers are available.

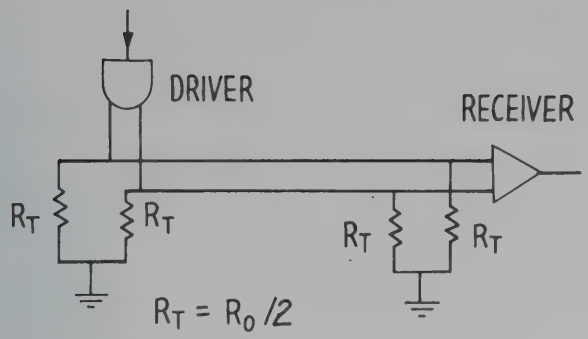



Figure 9.17. Differential Transmission Dual Termination

| | DIFFERENTIAL | SINGLE ENDED |
|---|---|---|
| COMMON MODE VOLTAGE | ± 3V TO ± 25V | |
| SENSITIVITY | ±10 TO ± 25mV | ±100 TO ±2000mV |
| RESPONSE TIME | 25 ns | 15 TO 60 ns |
| SUPPLY | ± 5V | +5, ± 12 |
| TYPICAL RECEIVERS | SN75152<br>SN75107/108<br>SN75207/208<br>SN75115<br>SN75182 | SN75140<br>SN75121<br>SN75123<br>SN75154 |

Figure 9.18. Summary of Receiver Properties

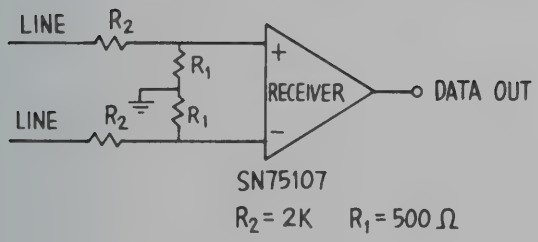



Figure 9.19. Input Attenuators to Increase Receiver Common Mode Limit

| | CONSTANT CURRENT OUTPUT | CONSTANT VOLTAGE OUTPUT |
|---|---|---|
| OUTPUT CURRENT | 6-12mA | 40-300mA |
| OUTPUT VOLTAGE | — | 2-30V |
| PROPAGATION DELAY | 8-25ns | 12-20ns |
| SUPPLY | ± 5V | +5V |
| TYPICAL DRIVERS | SN75109/110 | SN75114/113<br>SN75183<br>SN75450 SERIES |

Figure 9.20. Typical Driver Characteristics

**Single Supply Circuits – Differential Line Systems** **(Figure 9.21)**

The currently available single supply receivers are not as sensitive as those available in dual supply components; therefore, the line length and data rates attainable with such systems are less at present than those available with a dual supply system. With single supply systems, it's difficult to be specific about the operating frequency at specific line lengths because frequency and line length are so interdependent.

**Typical Differential System Performance** **(Figure 9.22)**

A system configuration similar to the configuration just discussed uses an SN75114 driver, an SN75115 receiver, and a twisted pair line with 5 turns per foot of No. 22 AWG wire. This system was successfully used at data rates to 1.5 mega bits/second and line lengths to 1000 feet.

**High Data Rate Single-Ended System – Single Supply** **(Figure 9.23)**

This shows a single-ended high performance system which uses an SN75450 or an SN75361 peripheral driver to achieve a data rate to 10 MHz over 100 feet of twisted pair line, using a single +5 volt system supply and an SN75154 line receiver.

**Example of Differential Line System** **(Figure 9.24)**

In order to achieve high bit rate transmission over long lengths it is necessary to use differential line circuits. This configuration is using an SN75107 receiver and an SN75109 driver in a system with the $R_T$ resistors connected to dc ground to achieve data rates of up to 20 MHz in lines over 100 feet long.

**Simple Party Line System** **(Figure 9.25)**

These same systems can be used for party line or multiway transmission if proper consideration is given to the procedures for selecting source destination station pairs and the procedure for accessing the party line. The basic party line configuration is shown here.

**Party Line System Control** **(Figure 9.26)**

There are three basic solutions to party line timing and control, as summarized in this table. The concept of the addressing approach is that the driver sends an address which is decoded by the receivers activating the desired driver for reply. The line busy indicator method is simply a logic to detect the presence of signals on the line with the logic output driving the driver inhibit terminal and a line busy indicator light.

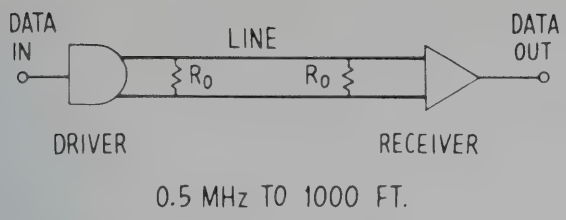



Figure 9.21. Single Supply Circuits – Differential Line Systems

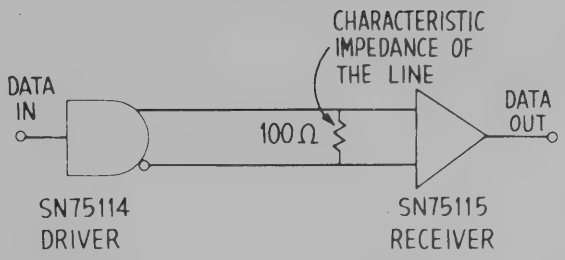



Figure 9.22. Typical Differential System Performance

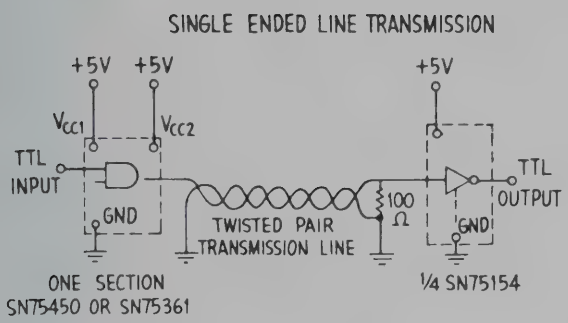



Figure 9.23. High Data Rate Single-Ended System – Single Supply

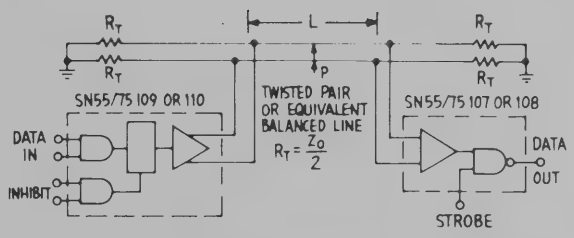



Figure 9.24. Example of Differential Line System

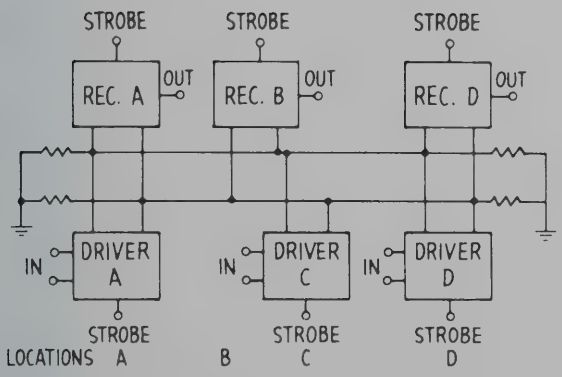



Figure 9.25. Simple Party Line System

- LINE BUSY INDICATOR AND DRIVER INHIBITOR
- TIME MULTIPLEXING
- ADDRESSING

Figure 9.26. Party Line System Control

**Data Terminal with Busy Inhibit** **(Figure 9.27)**

An example of such a line busy detector and control circuit is shown in this circuit block diagram. The first part of the logic detects if either a 0 or 1 is being sent, if either is, the line is in use and a flip-flop is set which inhibits the local driver and lights the line busy indicator. As soon as the line is free, indicating no further "0" or "1" on the line, the flip-flop is reset, a line available light is energized and the driver can be enabled by the user.

**Time Multiplexing System** **(Figure 9.28)**

The time multiplexing approach is easily implemented by adding a second transmission system to send the system timing signals on, as shown in this block diagram. In this example the system clock and driver select network allows a time sharing procedure so that in a given sequence the appropriate driver receiver pairs may transmit information for a period of time during each cycle period.

## SUMMARY

This session has covered the design relationship to enable the design of high performance systems and also provided an introduction to party line systems. This material should solve any data transmission problem, whether standard or special purpose, by proper choice of the transmission line, the line receiver, and the line driver.

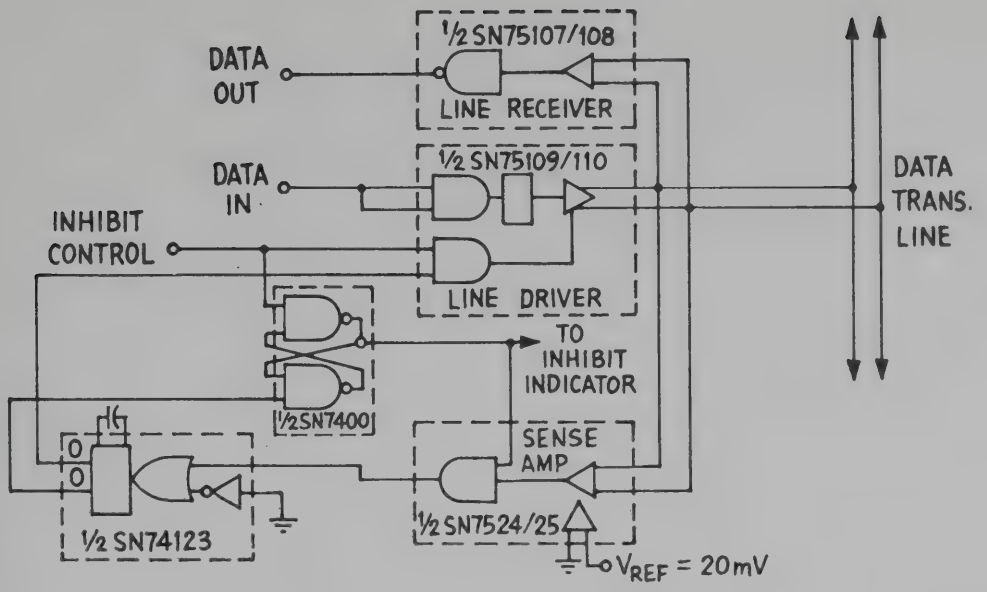



Figure 9.27. Data Terminal with Busy Inhibit

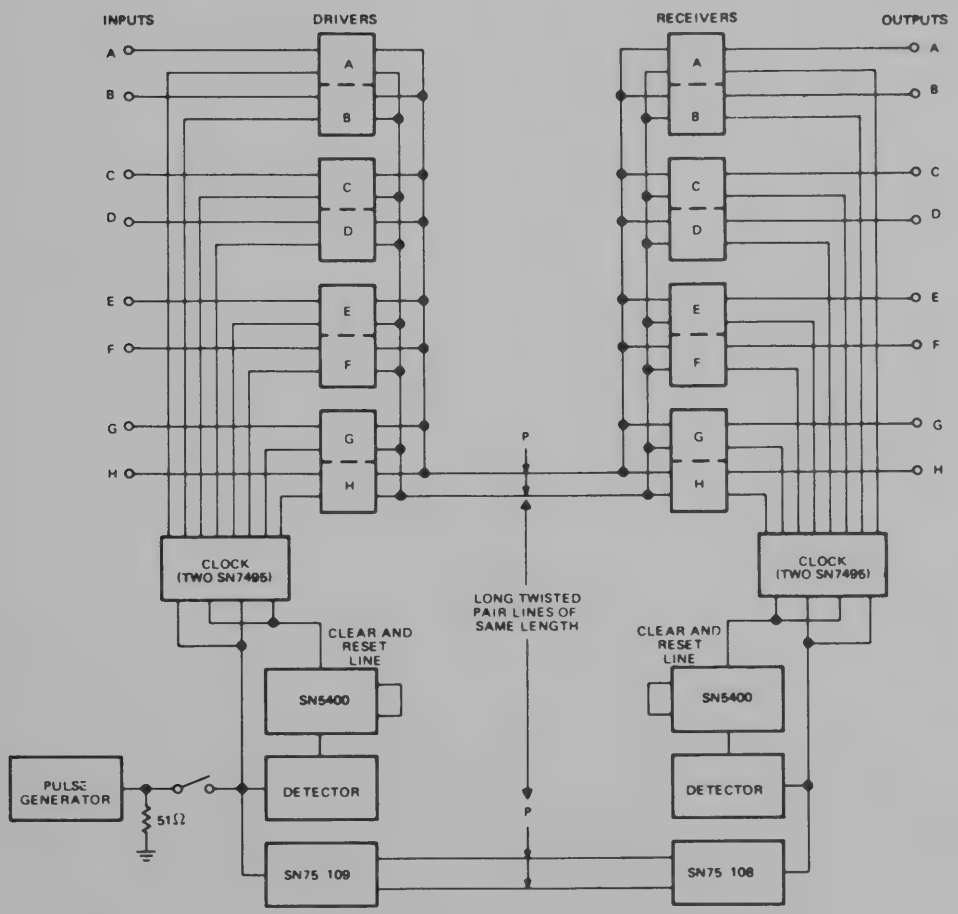



Figure 9.28. Time Multiplexing System

# Lesson 10

# DC VOLTAGE REGULATOR DESIGN

*Gives the important characteristics of dc voltage regulator integrated circuits. Discusses the means of generating the accurate reference voltages and the high gains required as well as the protection circuits.*

# Lesson 10

# DC VOLTAGE REGULATOR DESIGN

*A stable, high-gain linear dc integrated circuit amplifier has become the building block component of the linear system designer's workbook. This is the operational amplifier.*

*The design, processing and fabrication progress that has been made in operational amplifiers has made significant impact on another circuit requiring similar precision, the voltage regulator.*

*In this lesson the design of voltage regulators is discussed.*

**Functions of a Voltage Regulator** **(Figure 10.1)**

The output voltage is sampled and fed to a circuit to compare the sampled voltage to a reference voltage. If there is a difference, an error, it is amplified and applied to a control element to change the output voltage to reduce the error to zero.

**Voltage Regulator with Error Amplifier** **(Figure 10.2)**

Since the compare and amplifier function in most of the modern-day integrated circuit regulators is performed in one circuit, it is replaced with one block, an error amplifier.

**Equation Used to Determine Regulated Output Voltage** **(Figure 10.3)**

The output voltage change is a function of changes in input voltage, output current, the temperature of the components in the circuitry, and long-term changes with time.

The purpose of this lesson is to explain the function of voltage regulator elements and to indicate the design progress that has been made by the industry in the performance of these elements.

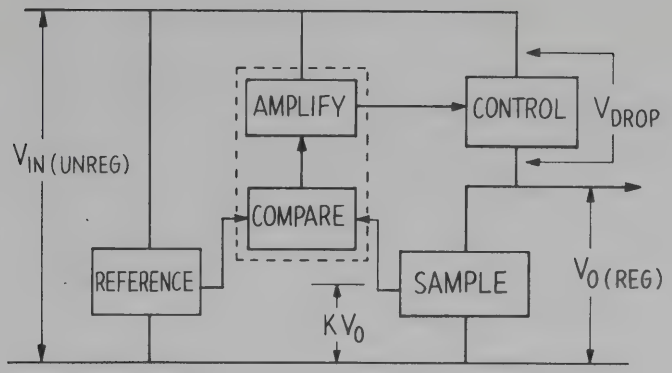



**Figure 10.1. Functions of a Voltage Regulator**

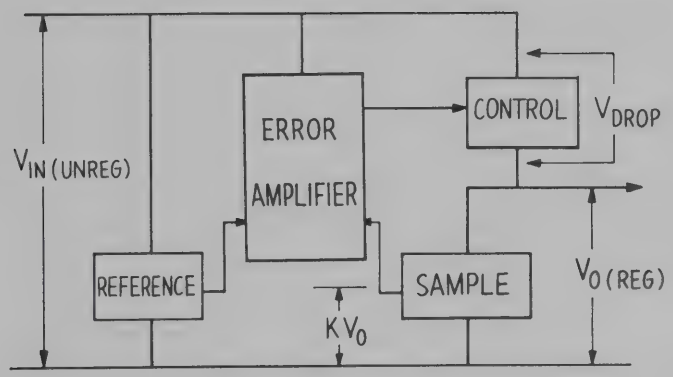



**Figure 10.2. Voltage Regulator with Error Amplifier**

TOTAL REGULATED VOLTAGE CHANGE | DUE TO INPUT V CHANGE | DUE TO LOAD I CHANGE | DUE TO TEMPERATURE CHANGE | DUE TO TIME

$$\Delta V_O = \Delta V_{O(\Delta V_I)} + \Delta V_{O(\Delta I_L)} + \Delta V_{O(\Delta T)} + \Delta V_{O(\Delta t)}$$

**Figure 10.3. Equation Used to Determine Regulated Output Voltage**

**Reference Element** **(Figure 10.4)**

Zener diodes, a standard for generating a constant voltage, are made satisfactorily in integrated circuit form, but, because of characteristics shown here – temperature coefficient and impedance changing with the value of the zener voltage and the output impedance varying with the bias current – special processing is required to control these characteristics.

Zener diodes tend to be noisy so that many regulators have external terminals for bypass capacitors.

**Voltage Divider Resistors and Buffer Stage** **(Figure 10.5)**

With the reference voltage source between 6 and 8 volts, additional resistor dividers must be used to regulate at a lower voltage than the primary reference voltage. These dividers are quite satisfactory, but the additional voltage drops due to reference load current variations contribute to larger regulation coefficients. Many regulators provide buffer stages, as shown here, to minimize the loading.

The key to a stabler and more integrable reference voltage is the use of forward base-emitter voltage of IC transistors.

**Reference Voltage Circuits** **(Figure 10.6)**

Shown are two circuits: The first combines temperature coefficients of the zener diode, the base-emitter diodes, and the resistors, to form a stable reference voltage which is now much lower than the zener voltage itself.

In the second circuit, even lower and more predictable reference voltages are possible. Such reference voltage sources are internally contained and are free from noise without bypass capacitors.

In operation, $I_1$ is 10 to 20 times the magnitude of $I_2$. Therefore, there is a delta $V_{BE}$ which appears across $R_3$ and sets the current $I_2$. $I_2R_2$ and the $V_{BE}$ of $Q_3$ provide a reference that stabilizes the output voltage to approximately 0.005%/°C. Once a stable reference is established, it can be compared with the sampled output, and the error can then be amplified to control the output voltage.

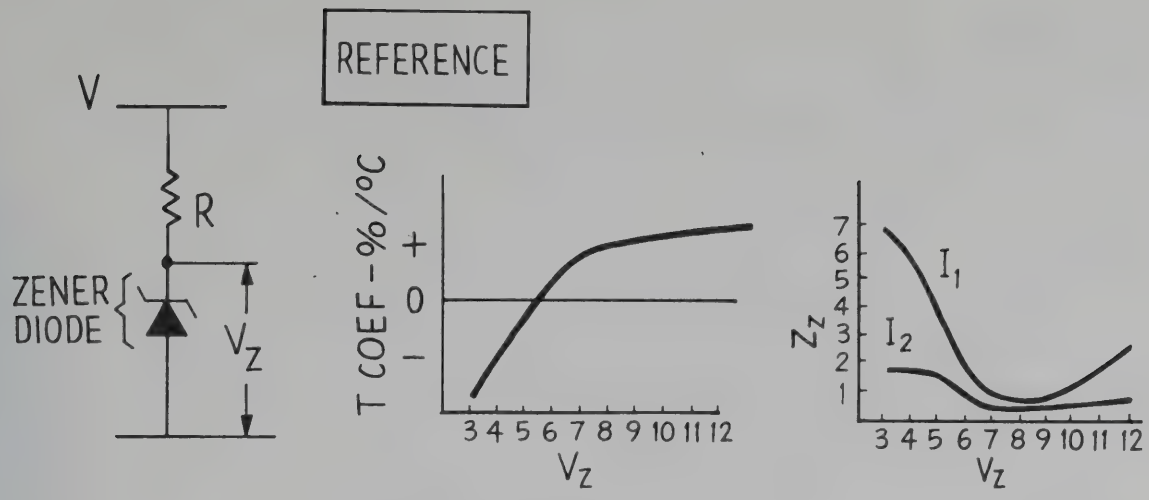



Figure 10.4. Reference Element

$V_O > V_{REF'}$

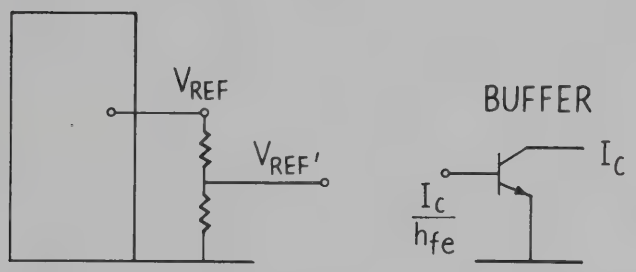
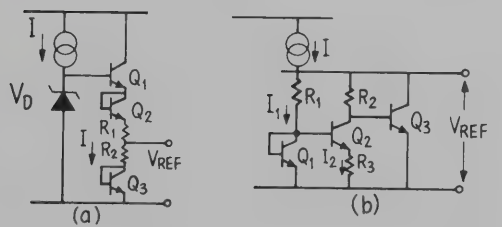



Figure 10.5. Voltage Divider Resistors and Buffer Stage

REFERENCE ELEMENT




$V_{REF} = IR_2 + V_{BE3}$

$V_{REF} = V_{BE3} + \frac{R_2}{R_3}\left(\frac{K_T}{q} \text{Ln} \frac{R_2}{R_1}\right)$

$$I = \frac{V_D - (V_{BE1} + V_{BE2} + V_{BE3})}{R_1 + R_2}$$

$$V_{REF} = \frac{R_2}{R_1 + R_2}(V_D - V_{BE1} - V_{BE2} - V_{BE3}) + V_{BE3}$$

$$V_{REF} = \frac{R_2}{R_1 + R_2}\left[V_D - V_{BE1} - V_{BE2}\right] + V_{BE3}\left[1 - \frac{R_2}{R_1 + R_2}\right]$$

Figure 10.6. Reference Voltage Circuits

**Sampling Element** **(Figure 10.7)**

The sampling element in most cases is a resistive divider, either fixed or adjustable as shown in the figure, but it can be a series of diode drops developed with a current as shown here.

**Error Amplifiers** **(Figure 10.8)**

An early discrete component error amplifier is shown on the left. An increase in output voltage was sensed as an increase in $V_{BE}$ of $Q_1$ which increased $I_1$, decreased $I_2$, and increased the drop from $V_1$ to $V_0$ to compensate and reduce the output voltage. Such regulators provided ±2% voltage regulation.

A modern-day voltage regulator error amplifier is shown on the right of Figure 10.8. The output voltage sample is compared against reference voltage and appears as an error in $V_{BE3}$.

Through the employment of large load impedances, amplifiers (usually with multiple stages) can have gains approaching 100,000. Resistors of this size are very difficult to make using diffusion techniques. However, simulating the conditions with an active device provides a very cost-effective solution.

**Control Element** **(Figure 10.9)**

The control element has an input voltage that is larger than the output voltage, and has some means of driving or controlling the element. Control by a current in parallel with the load is called "shunt control." If the control current is in series with the load, then it is a "series control" element.

The series regulator must handle the full load current, but the voltage across the element, $V_I - V_O$, can be much less than the output voltage. It has a maximum internal power dissipation at full load.

The shunt regulator has the full output voltage across the element. The series dropping resistor has continuous high dissipation, and degrades the efficiency of the regulator. The shunt regulator has maximum internal power dissipation at no load.

Striving for maximum efficiency and lowest power dissipation, IC regulators use series control elements. The most limiting factor with IC regulators is high temperature.

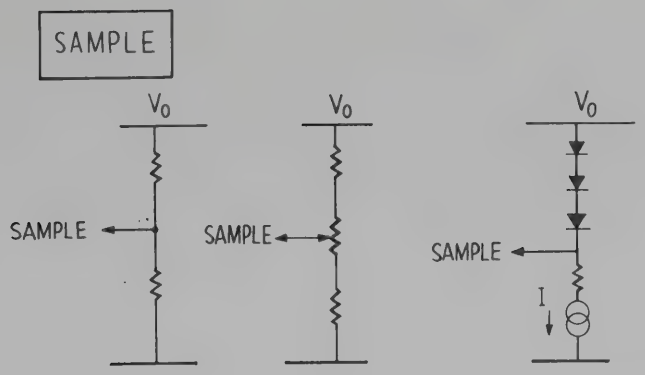



Figure 10.7. Sampling Element

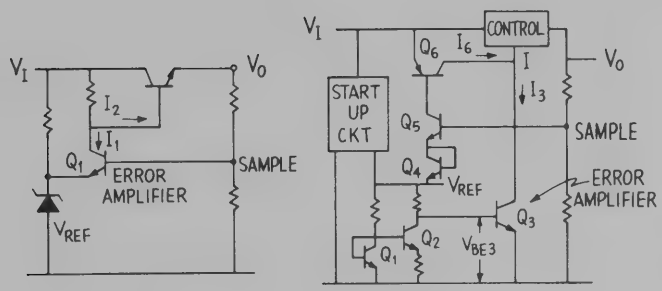



Figure 10.8. Error Amplifiers

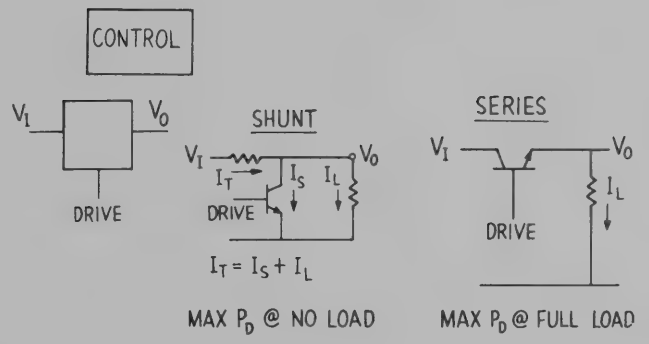



Figure 10.9. Control Element

**Maximum Junction Temperature** **(Figure 10.10)**

As shown in the illustration, the maximum junction temperature results from the surrounding ambient temperature plus the rise in temperature due to the power dissipation, which is represented here as the power dissipation times the thermal resistance from junction to ambient. $\theta_{JA}$ may be separated into its parts of junction-to-case, case-to-heatsink, and heatsink-to-ambient.

The power dissipation, $P_D$ can be expressed as the input voltage times the standby current plus the power dissipated because of a load which is the drop across the control element times the load current.

With the load current up to hundreds of milliamperes and the standby current in milliamperes, the major portion of the internal temperature rise is due to the dissipation of the series control element.

However, an even greater limiting factor on the maximum current of the regulator is the physical size of the control element.

**IC Regulator Chip** **(Figure 10.11)**

For example, a picture of an IC regulator chip is shown in the figure. The series control element transistor occupies more than 50% of the chip area. Therefore it limits the cost effectiveness of a design. All the elements of the regulator have now been covered.

**IC Regulators** **(Figure 10.12)**

Shown is a list of integrated circuit regulators offered, or to be offered, by Texas Instruments. Also listed are the input voltage limits, the output voltage and current limits, and the type of package or case.

$$T_{J(MAX)} = T_A + T_{JA}$$
$$= T_A + P_D \theta_{JA}$$
$$= T_A + P_D (\theta_{JC} + \theta_{CA})$$
$$= T_A + P_D (\theta_{JC} + \theta_{C-HS} + \theta_{HS-A})$$

$$P_D = V_I \times I_{STANDBY} + (V_I - V_O) I_L$$

Figure 10.10. Maximum Junction Temperature

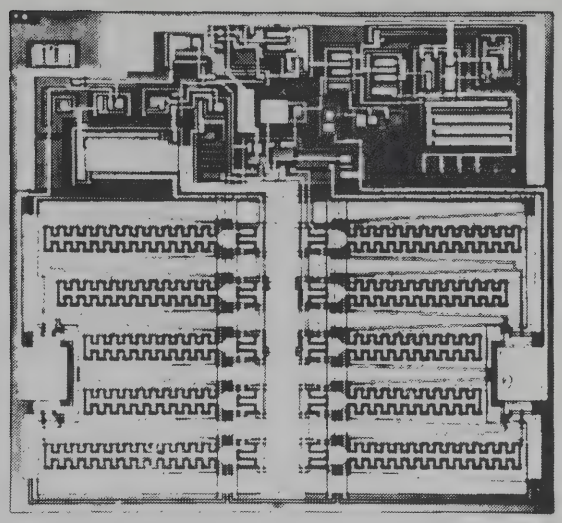


Figure 10.11. IC Regulator Chip

| DEVICE | INPUT V | OUTPUT V | OUTPUT I | PACKAGE |
|---|---|---|---|---|
| SN52/72723 | 9.5-40 | 2-37 | 0-150 mA | JNL |
| *SN52/72401 | 9.5-40 | 2.5-28 | 0-150 mA | JN |
| SN52/72403 | 9.5-40 | 2.5-37 | 0-150 mA | LP |
| *SN52/724xx | 0.5-40 | 5-24 | 0-150 mA | L,P |
| **SN52109 | 7-25 | 5±0.3 | 0-200 mA | L (TO-5) |
| **SN72309 | 7-25 | 5±0.2 | 0-500 mA | L (TO-5) |
| SN52109 | 7-25 | 5±0.3 | 0-1 A | TO-3 MC |
| SN72309 | 7-25 | 5±0.2 | 0-1.5 A | TO-3 MC |
| SN52104 | −8- −50 | 0- −40 | 0-20 mA | L |
| SN72304 | −8- −40 | 0- −30 | 0-20 mA | LN |
| SN52105 | 8.5-50 | 4.5-40 | 0-12 mA | L |
| SN72305 | 8.5-40 | 4.5-30 | 0-12 mA | LP |
| SN72305A | 8.5-50 | 4.5-40 | 0-45 mA | LP |
| SN72376 | 9-40 | 5-37 | 0-25 mA | LP |
| SN52900 | 7-40 | 5-24 | 0-200 mA | L |
| SN72900 | 7-40 | 5-24 | 0-200 mA | LP |
| **7805 | 7-25 | 5±0.2 | 0-1.5 A | TO-66 P |
| **7806 | 8-25 | 6±0.25 | 0-1.5 A | TO-66 P |
| **7808 | 10.5-25 | 8±0.3 | 0-1.5 A | TO-66 P |
| **7812 | 14.5-30 | 12±0.5 | 0-1.5 A | TO-66 P |
| **7815 | 17.5-30 | 15±0.6 | 0-1.5 A | TO-66 P |
| **7818 | 21-33 | 18±0.7 | 0-1.5 A | TO-66 P |
| **7824 | 27-38 | 24±1.0 | 0-1.5 A | TO-66 P |

*EXPERIMENTAL UNITS
**FIXED OUTPUT VOLTAGES

Figure 10.12. IC Regulators

**Regulator Coefficients** **(Figure 10.13)**

The range of regulation coefficients for the above regulators is 0.05 to 0.2% for line regulation; 0.05 to 0.5% for load regulation; 0.3 to 1% for 100°C change in ambient temperature and 0.1 to 1% for long term drifts based on a 1000-hour time period.

The line regulation is for at least a 3-volt change in input voltage, the load regulation is from no load to full load current, and the temperature change as shown is 100°C.

Additional circuits added for protection of the regulator may be classified as follows:

1) Current Limit
2) Thermal Protection
3) Safe Area Protection
4) Other Protection.

**Current Limit** **(Figure 10.14)**

Shown are several circuits that are used to protect a regulator from damage due to a short on the output. The short-circuit current, $I_{SC}$, flows through a resistor in series with the output which develops a voltage across it. $Q_1$ conducts when the voltage is greater than threshold $V_{BE}$, and reduces the drive on the series control element. The series transistor absorbs the $V_I - V_O$ drop and limits the current to $I_{SC}$. $R_{SC}$ in some cases is included on the IC chip.

The foldback protection circuit reduces the value of the short circuit current from a value of $I_K$ at the knee of $V_O$ to a value $I_{SC}$ when $V_O$ equals zero. Resistors $R_1$ and $R_2$ are not generally included on the chip, allowing for flexibility in setting the foldback limit.

**Thermal Protection** **(Figure 10.15)**

To prevent thermal runaway, the thermal protection circuit shown is sometimes provided. Such a circuit does not operate until the junction temperature of the series control element reaches a predetermined value. Two such circuits are shown. They both reduce the drive on the series control element so that dissipation is limited.

A significant advantage for monolithic regulators is that such circuits allow the $I_{SC}$ at normal operating conditions to be higher than it would be without the thermal protection circuit, because $I_{SC}$ would be derated to stay within power dissipation limits.

| $\Delta V_O(\Delta V_I)$ | $\Delta V_O(\Delta I_L)$ | $\Delta V_O(\Delta T)$ | $\Delta V_O(\Delta t)$ |
|---|---|---|---|
| LINE | LOAD | TEMPERATURE | TIME |
| 0.05-0.2% | 0.05-0.5% | 0.3 TO 1% FOR 100°C | 0.1 TO 1% |

Figure 10.13. Regulator Coefficients

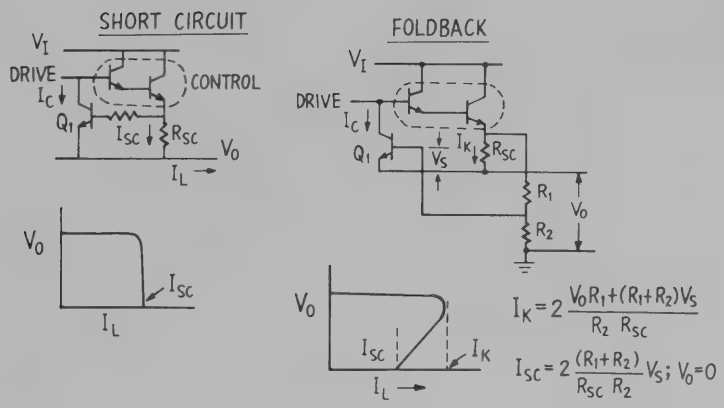



Figure 10.14. Current Limit

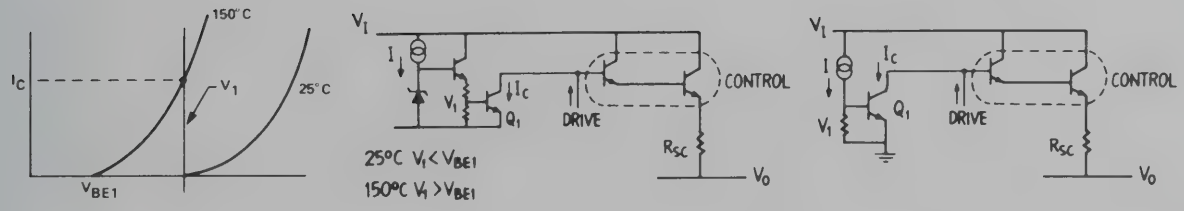



Figure 10.15. Thermal Protection

**Typical Protection Circuit for Excess Voltage** **(Figure 10.16)**

Shown is a typical protection circuit for excess voltage. The resistor $R_1$ and the zener diode $D_1$ form the circuit. When the differential voltage across the series control element is a safe value, there is only a very small current through $R_1$ and $D_1$. Exceeding the safe value causes significant current to flow which has the effect of reducing the limit current, $I_{SC}$, in the series element. Such protection is called "forward safe area protection."

Other protection circuits may be incorporated in some of the regulator designs, or they may be easily provided externally.

**Other Protection** **(Figure 10.17)**

A list of these is shown in the figure. Compensation is either internally provided, or terminals are available for it externally. Values of 20 to 100 pF are normal compensation capacitances. Compensation determines the speed of response.

Input voltage transients, reverse input and output polarity, and excessive output voltage are controlled by either forward or zener diodes internally or externally. However, one protective feature somewhat peculiar to monolithic regulators is that of load protection. If the series transistor shorts, this, of course, ruins the regulator but the chip metallization usually fuses open to protect the load.

**3-Terminal Regulator** **(Figure 10.18)**

This is an example of a 5-volt regulator for logic circuits. It needs no external components, has all the protection circuits, and provides excellent regulation. Similar regulators are available from 5 to 24 volts in convenient DIP packages.

**SN52/72403 Voltage Regulator** **(Figure 10.19)**

Shown is an 8-pin dual-in-line packaged regulator, the SN52/72403. The unit is easy to use. It can be dropped into the socket, or soldered into the board. Pins 6, 7 and 8 are shorted, pin 4 is tied to ground. The divider $R_1$ and $R_2$ is placed between pin 5 and ground in the correct ratio for the output voltage chosen. The junction of $R_1$ and $R_2$ is tied to pin 3, the input voltage $V_I$ is applied and the output voltage is taken from pin 5. The regulation for line variation is 0.1%, 0.15% for load variation, and 0.015%/°C for temperature.

**SUMMARY**

This lesson has discussed the elements of a regulator, showed the trends in design, and some of the circuit details. As with other linear ICs the advances have been significant in the last several years. The limitation of power dissipation, silicon area and packaging will certainly be overcome with similar innovations in the future.

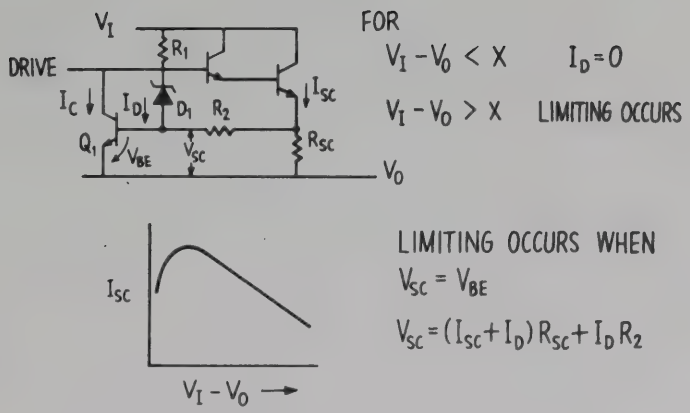
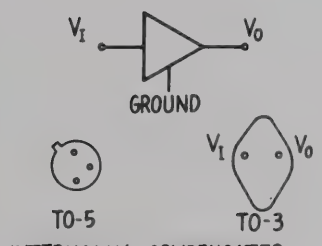



**Figure 10.16. Typical Protection Circuit for Excess Voltage**

## OTHER PROTECTION

1. AC COMPENSATED
2. INPUT VOLTAGE REVERSING POLARITY
3. EXCESSIVE OUTPUT VOLTAGE
4. PROTECTION OF LOAD BY FUSING METAL ON I/C CHIP

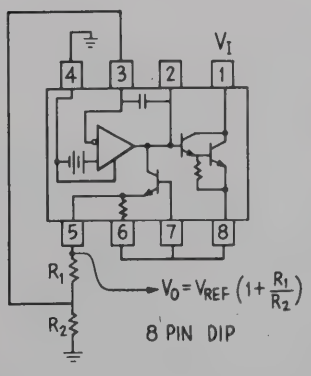
**Figure 10.17. Other Protection**




INTERNALLY COMPENSATED
NO EXTERNAL COMPONENTS
INTERNAL THERMAL OVERLOAD
SHORT-CIRCUIT CURRENT LIMIT
SAFE-AREA PROTECTION

SN52109 -55°C -125°C
SN72309 0° -70°C
$V_O$ - 5V ± 0.2V
$I_L$ - 0.2 - 1.5A
$\Delta V_{O(\Delta V_I)}$ = 4mV - 0.08%
$\Delta V_{O(\Delta I_L)}$ = 30mV - 0.6%
$\Delta V_{O(\Delta T)}$ = 20mV - 0.4%

**Figure 10.18. 3-Terminal Regulator**




$V_O$ - 2.5 TO 29 VOLTS
$V_I$ - 9.5 TO 32 VOLTS
ADJUSTED WITH EXTERNAL DIVIDER
LINE REG. 0.1%
LOAD REG. 0.15%
TEMP STAB 0.015%/°C
$I_{SC}$ = 80 mA
$I_L$ = 1 - 150 mA
$P_D$ = 800mW @ 25°C
DERATE 6.4mW/°C
SN52403 - 55°C TO + 125°C
SN72403 0°C TO + 70°C

**Figure 10.19. SN52/72403 Voltage Regulator**

# Lesson 11

# VOLTAGE REGULATOR APPLICATIONS

*The range of application of integrated circuit regulators to various voltage and current conditions is defined. The coefficients contributing to output voltage change are defined and demonstrated.*

# Lesson 11

# VOLTAGE REGULATOR APPLICATIONS

*The purpose of this lesson is to review the principles of operation of an integrated circuit voltage regulator.*

**Representative Power Supply Configuration** **(Figure 11.1)**

This shows ac power into a transformer, rectifier, and filter that produce unregulated dc voltage with a slight ripple. The IC voltage regulator uses a series pass transistor to regulate the dc voltage, keeping the output voltage relatively constant despite changes in the load.

**Performance Graphs** **(Figure 11.2)**

Shown are several different parameters plotted with respect to time with the time scale being greatly compressed at the right end. At the top is the desired output voltage, $V_O$. The jagged line is an amplified exaggeration of the actual output voltage. There is a prominent transient negative spike caused by a sudden change in the load current.

Specifications for the 3 "high frequency" aspects of voltage regulator behavior are ripple rejection ratio (in decibels), noise voltage at constant load current and temperature, and turn-on and turn-off times for specified step-function changes in load current or input voltage. These factors are dependent on the frequency response of the error amplifier compensation.

The broken line is the dc component of the output voltage. It is subject to variation due to four main factors which are: load current ($I_L$), temperature of the semiconductor element, input of "line" voltage ($V_I$), and time.

The long-term drift in time shown in the compressed section of the time scale is usually expressed as a percentage change over a certain period, usually a thousand hours. The voltage increase on the right side in Figure 11.2 is in response to the step in input shown immediately below. The voltage decrease at the left of Figure 11.2 is due to the sudden change in load current. Due to the increased load current and the power dissipation, chip temperature rises. As a result, the output voltage changes.

These seven aspects of performance are not independent of each other, but are iterrelated in various ways.

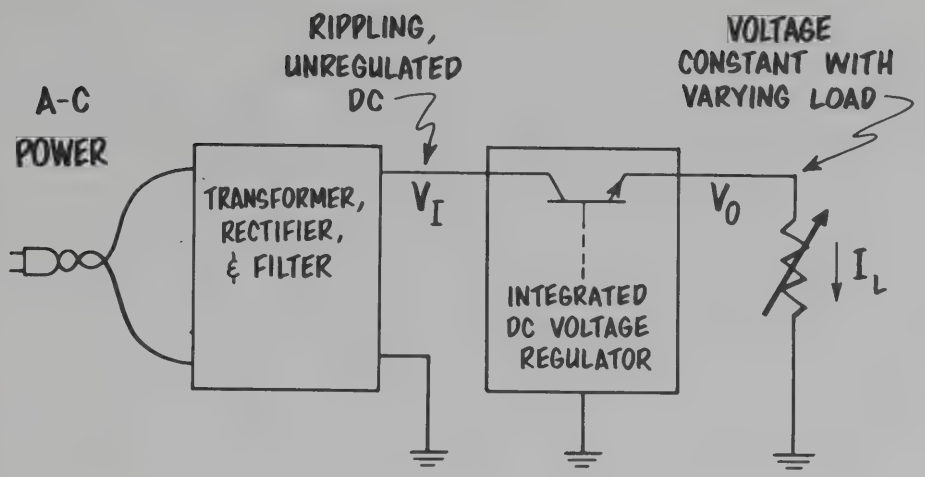



Figure 11.1. Representative Power Supply Configuration

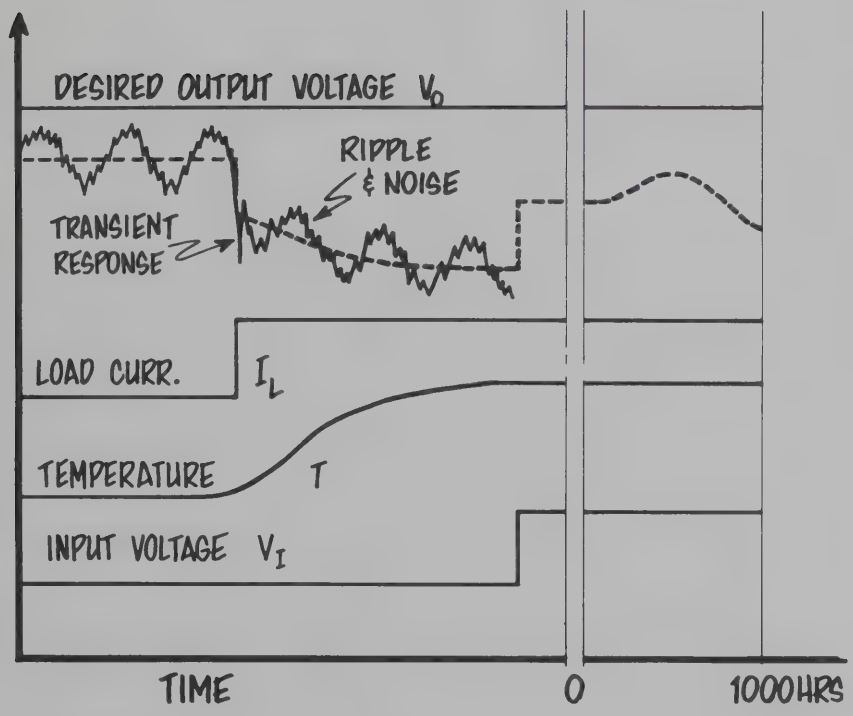



Figure 11.2. Performance Graphs

**Voltage Regulator Circuit** **(Figure 11.3)**

Here a transformer, rectifier, and filter (not shown) are supplying dc at about 15 to 17 volts, depending on the load. The output voltage is set at five volts. A 50-Ω load is connected through a switch, and through a current meter to ground.

The SN72403 is symbolized by the darker rectangle and contains a series-pass transistor, a driver transistor, and internally compensated error amplifier, and a 2.5-volt reference-voltage circuit plus some current-limiting circuitry not shown.

Outside the IC are resistor dividers $R_1$ and $R_2$, providing a sense voltage to the error amplifier. These resistances are equal so that the error amplifier tries to maintain the output at twice the reference voltage or five volts.

The load regulation capability for a change in load may be computed by using the formula:

$$\text{change} = \frac{\text{E change}}{\text{E out}} \quad \text{X } 100.$$

An important consideration is the temperature coefficient of the voltage regulator circuit. As current is drawn from the supply, the temperature of the chip increases, which causes the output voltage to decrease. Heat-sinking the regulator would have helped in maintaining the desired five volts of output.

**Voltage-Regulator Circuit with Series Transistor** **(Figure 11.4)**

The current-handling capability of the circuit can be boosted by adding a power transistor to the output. The effective series-pass element is now a TIP-31. The series transistor in the IC serves as the driver for the TIP-31. The sense network still senses the output voltage. A change in the load to about 6.25 Ω will give us about 800 milliamps of load current.

The output voltage with no load applied is approximately 5 volts. When the load is applied the output voltage falls under these conditions, and the voltage regulation percentage is approximately the same as when only 100 milliamps of load current was flowing without the power transistor. The load-handling capability of the regulator was increased by a factor of eight.

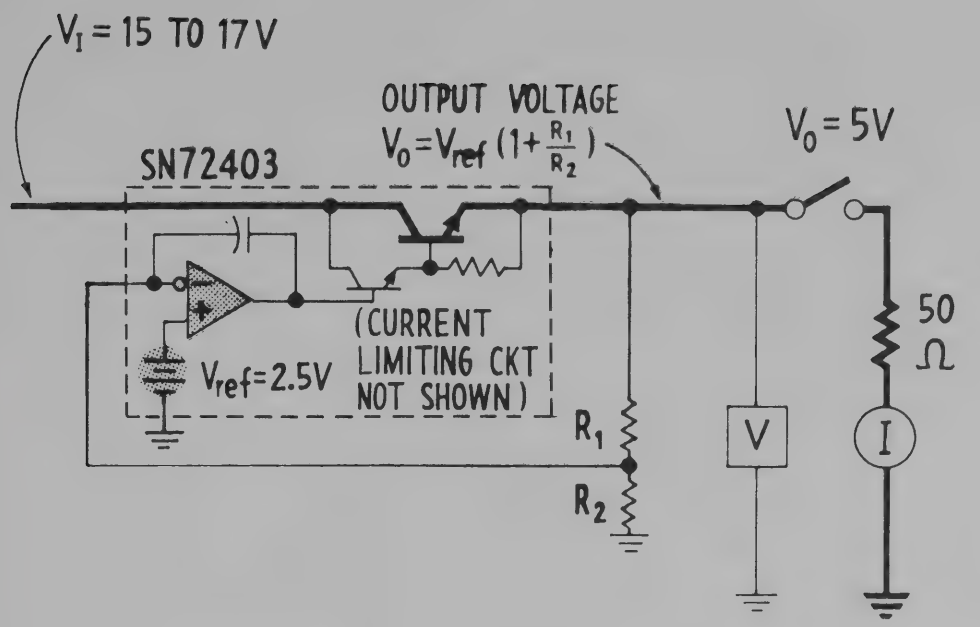



Figure 11.3. Voltage Regulator Circuit

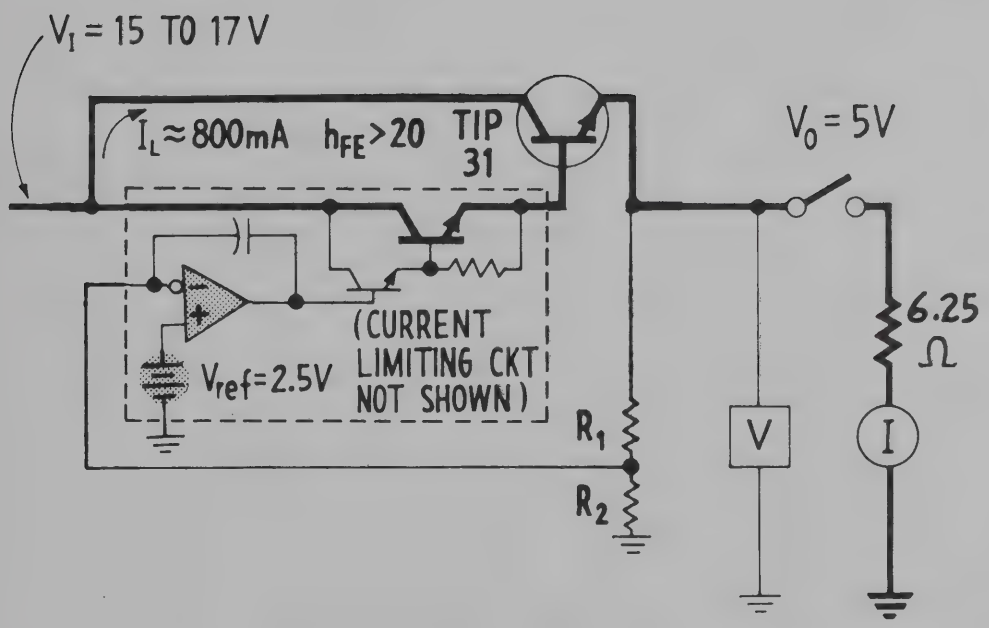



Figure 11.4. Voltage-Regulator Circuit with Series Transistor

**Voltage-Regulator Circuit with Switching Transistor Load** **(Figure 11.5)**

The load can be replaced with a switching circuit in series with a 100-ohm load resistor, allowing a load current of 50 milliamps. The transistor, operated in saturation, may be used to turn the load current on and off under the control of a pulse generator.

An oscilloscope may be connected on both sides of the 100 Ω resistor to show two waveforms simultaneously. The upper trace on the scope face will show output voltage; the lower trace indicates the magnitude of the load current.

The switching transistor is pulsed at a frequency of 100 kHz, with a 50% duty cycle.

**Scope Face Showing Transient Response** **(Figure 11.6)**

The scope face shows the output voltage on its top trace; bottom trace indicates the magnitude of the load current. The tops of the square waves indicate zero current for a duration of 5 microseconds.

The bottom of the square wave indicates a load current of 50 milliamps for a duration of 5 microseconds. The rapid turn-on and turn-off of the load current produce a "spike" voltage that has a duration of more than 1 microsecond. This output variation is indicative of the transient response of the voltage regulator.

**Voltage-Regulator Circuit with 100 Ω Resistor Parallel to Load** **(Figure 11.7)**

Transients can be reduced by keeping the load current from dropping to zero. With another 100 Ω resistor connected in parallel, the load will be switched between 50 and 100 milliamps rather than between 0 and 50 milliamps.

**Scope Face Showing Improved Transient Response** **(Figure 11.8)**

The top of each wave represents 50 milliamps of load current and the bottom stands for 100 milliamps rather than 0 and 50 as was achieved earlier. As a result, the transients in the output voltage are greatly reduced and thus easier to filter.

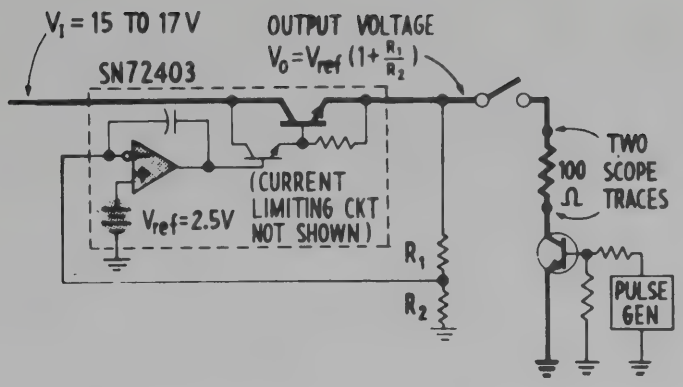



Figure 11.5. Voltage-Regulator Circuit with Switching Transistor Load

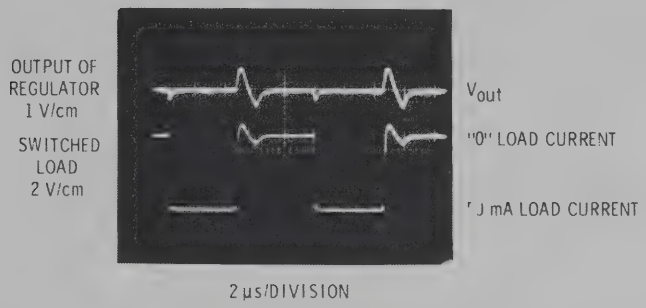



Figure 11.6. Scope Face Showing Transient Response

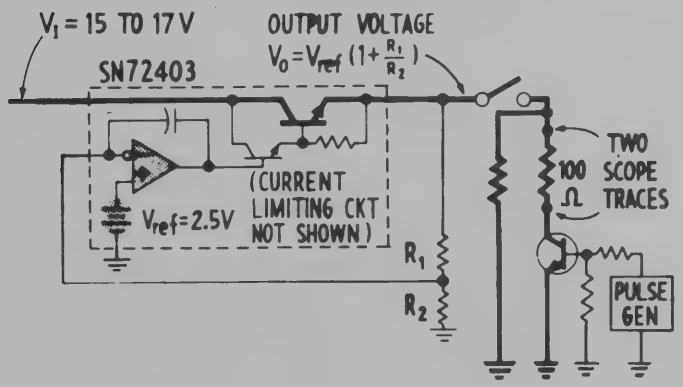



Figure 11.7. Voltage-Regulator Circuit with 100 Ω Resistor Parallel to Load

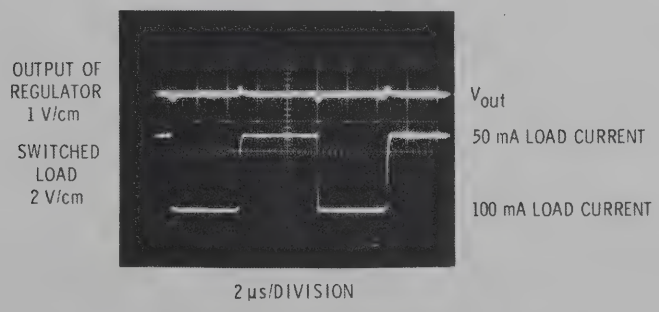



Figure 11.8. Scope Face Showing Improved Transient Response

**Laboratory Power Supply** **(Figure 11.9)**

A laboratory power supply can be built using the SN72403 as the regulating element controlling several different output voltages. If the desired outputs are 5 volts, 15 volts and 27.5 volts, current limitation must be employed in order to prevent overheating in the series-pass element. Current limitation is accomplished by a transistor that shunts drive current away from the series-pass transistor whenever the voltage drop across one of the series resistors exceeds about 0.4 volt – due to excessive load current passing through the resistor. The higher the output voltage, the more current the supply can stand, because the voltage drop across the series-pass transistor is low when the output voltage is high.

**Multiple Regulators with Emitter Grounded** **(Figure 11.10)**

Caution must be exercised when supplying several different voltage regulators from the same power source. A general representation of this situation appears in this figure.

The transformer secondary, the rectifier bridge, and the filter capacitor supply 20 volts of dc, with the positive side being the upper bus and the negative side being the lower bus. On the right are two regulators, showing the series-pass transistors, each having a separate load.

To obtain a 0 to –5-volt supply for the left-hand load, the ground connection must be attached to the emitter of the first regulator as shown. The 0 to –5 volts that was desired for the left-hand load has been achieved; however, this has thrown the other regulator into a rather strange configuration, with its load operating between ±5 volts.

**Multiple Voltage-Regulated Supply** **(Figure 11.11)**

Several regulated voltages, both positive and negative, are desired from the same transformer; a "negative" voltage regulator for each negative voltage must be supplied.

In this figure, the circuit must have one positive supply bus and one negative supply bus with a common ground. Power comes from two separate transformer secondary windings, bridges, and filter capacitors. Two SN72403s are shown supplying +5 and +10 volts to their loads. The 403 is called a "positive" voltage regulator, intended for use on the positive side of its load.

Down below are two negative voltage regulators, type SN72304, supplying –5 volts and –10 volts. This is a relatively simple way to handle multiple positive and negative voltages.

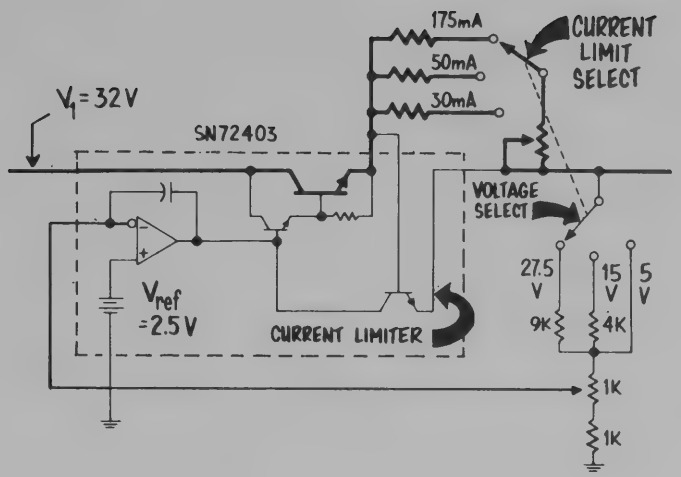



Figure 11.9. Laboratory Power Supply

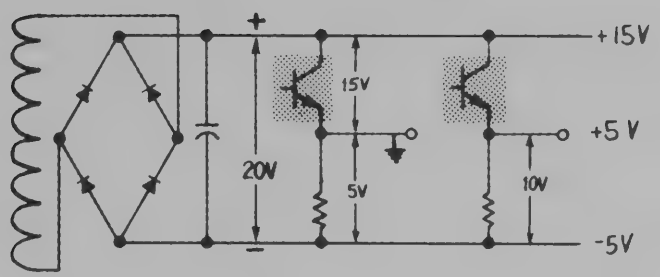



Figure 11.10. Multiple Regulators with Emitter Grounded

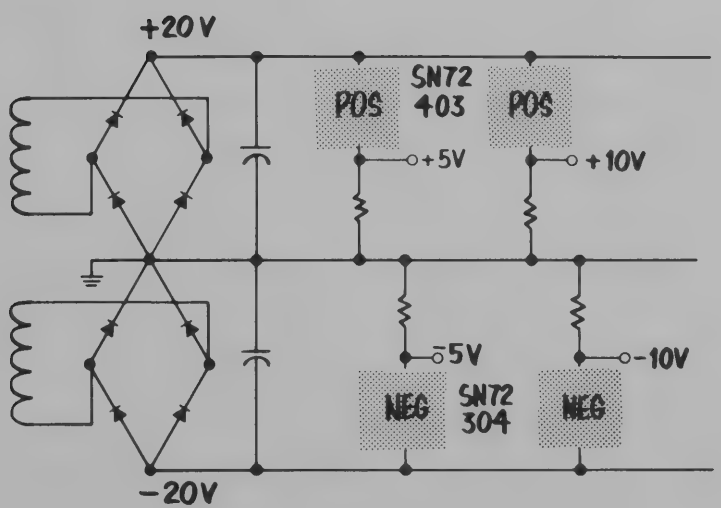



Figure 11.11. Multiple Voltage-Regulated Supply

**Regulated Supply with SCR Protection (Crowbar Circuit)** **(Figure 11.12)**

An important consideration is the protection of the load from catastrophic surges in the regulated voltage due to some sort of failure in the regulator circuit. A good overvoltage protector arrangement is shown in the figure.

The voltage regulator has a fuse in the input line. Regulated voltage is supplied by the bus to the load, which is now shown. An SCR is used to short out the regulator and blow the fuse when the voltage exceeds a certain threshold as sensed by the SN72560 precision level detector. The capacitor filters out transients, with a time constant of around 10 to 20 microseconds. There's a terminal on this IC which is not shown, where an external reference voltage can be applied.

## SUMMARY

The seven chief performance specifications studied will help choose from the very useful variety of ICs now available. Both positive and negative regulators are available. Some are called "programmable" regulators, with a number of sensing resistors contained within the IC. In the varied selection of useful regulators there are even regulators with only three terminals; namely, input, output, and ground with fixed sensing resistors contained in the IC.

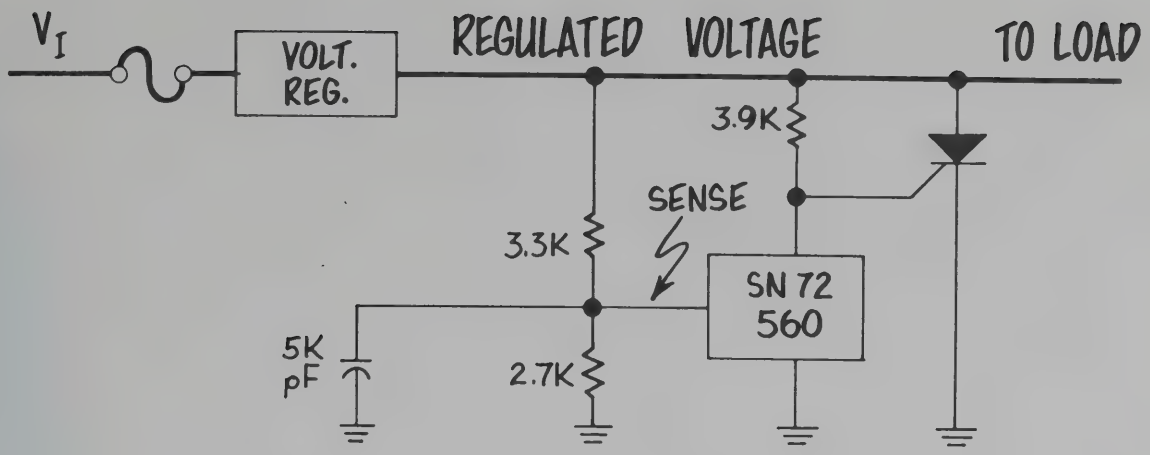



Figure 11.12. Regulated Supply with SCR Protection (Crowbar Circuit)

# GLOSSARY

**Active bandpass filter, 2-pole**

A circuit for selectively modifying the frequency response of an amplifier to provide a bandpass characteristic.

**Active load resistors**

Active devices that are used to electrically simulate a high value resistance in a small IC area (i.e., pinch resistor, collector FET resistor).

**AGC**

Abbreviation for automatic gain control. Circuit feedback connection for controlling the amplification of a circuit.

**$A_V(s)$ – Large signal voltage gain**

$A_V$ is the open-loop voltage gain as a function of frequency of the operational amplifier with external feedback connections removed. ($s = j\omega$)

**$A_{Vf}(s)$**

Closed-loop gain of the operational amplifier as a function of frequency. ($s = j\omega$)

**Bandwidth**

Range of frequencies considered to be the response range of a circuit. Normally is determined by assigning upper and lower frequency limits to be 3 dB below center frequency response level.

**$\beta(s)A_V(s)$**

The loop gain measured as a function of frequency around the complete feedback circuit; i.e., the gain of the feedback network $\beta(s)$ times the operational amplifier open-loop gain $A_V(s)$. ($s = j\omega$)

**B-H curve**

A graph representing the hysteresis loop of a material. It represents the flux density, B, produced as a function of the force, H, on a material.

**Binary coded decimal (BCD)**

A binary numbering system for coding decimal numbers in groups of 4 bits. The binary value of these 4-bit groups ranges from 0000 to 1001, and codes the decimal digits "0" through "9." To count to 9 takes 4 bits; to count to 99 takes two groups of 4 bits; to count to 999 takes three groups of 4 bits, etc.

**Bootstrapping**

This is a method of increasing the input impedance of an amplifier. Usually this is accomplished by feeding back a portion of the output signal in a direction that is opposite to the input signal current which results in less signal current in the input circuit, thereby making the input impedance higher.

**Chopper-stabilized operational amplifier**

An operational amplifier using chopper stabilization for low offset voltage drift and low current drifts.

**Chopper stabilization**

A means of signal processing in an amplifier that involves a low frequency signal path that has the dc and very low frequency components converted to a high frequency ac signal by the use of a chopper which is an electronic circuit that opens or shorts to ground the signal path.

**Clamp circuit**

A circuit designed to limit or restrict a signal voltage to a preset value.

**Coaxial lines**

Constant impedance shielded transmission lines with center conductors, flexible insulator, and outer shield conductor.

**Coincident current memory**

This is a memory unit that has read or write magnitudes of current adding at coincident times for selection of storage bits. Opposition of these currents determines the binary state of the information stored.

**Collector FET resistor**

Simplified pinch resistor using an isolated strip of n-type epitaxial material as the channel rather than a separately diffused p-type channel as used in the pinch resistor.

**Common mode rejection ratio (CMRR)**

The ratio of the differential voltage amplification to the common mode voltage amplification.

**Comparator (differential comparator)**

A differential-input, single-ended output, high-gain amplifier operating in the nonlinear region that is used to compare an analog signal applied to one of its input terminals to a reference voltage applied to its other input terminal. The output will be a digital one or zero when one input is higher than the other.

**Comparator strobe**

A terminal which permits the activation of the comparator's output stage for a given time interval.

**Complementary MOS (CMOS)**

A fabrication process for MOS which combines both p-channel and n-channel transistors on the same substrate. Only one transistor of the pair is normally on, except during the switching mode.

**Control element**

With reference to voltage regulators, it is the portion of the total circuit responsible for adequately compensating to keep the output voltage constant. The amplified error signal usually controls the control element.

**Core memory drivers**

Specially designed interface circuits used to drive inductive loads that provide high current, good high frequency response, and good breakdown voltage characteristics.

**Crossover distortion**

The deviation of an ac output signal from a linear relationship to the input signal at the time that the instantaneous signal crosses the zero axis.

**Data transmission system**

A system used for transmitting and receiving digital data along single wire, coaxial, or twisted pair transmission lines.

**Dielectric isolation**

The isolation of integrated circuit elements by separating them with a film of dielectric, usually silicon dioxide.

**Differential amplifier**

A direct-coupled amplifier that has both a differential input and a differential output.

**Differential input chopper (DIC)**

The DIC is the input circuitry of the chopper channel of a chopper stabilized operational amplifier.

**Diffused resistor**

An integrated circuit component formed by a diffusion process. The design of the resistor is primarily dependent on its geometry.

**Diode-biased transistor**

A simple form of current source using a transistor with its base and collector shorted in conjunction with another transistor with identical characteristics in order to match collector currents.

**Display drivers**

Solid-state drivers for energizing optoelectronic displays, specifically VLEDs.

**Dynamic storage elements**

Storage elements which contain storage cells that must be refreshed at appropriate time intervals to prevent the loss of information content.

**ECL circuits**

Bipolar emitter-coupled logic circuits, also called current-mode logic circuits.

**Epitaxial-collector resistor**

Built much like the collector-FET but without the gate diffusion across the top; basically an isolated strip of n-type epitaxial material with contacts at each end.

**Epitaxial growth**

The deposition of a monocrystalline layer of material onto a substrate material such that the layer thus formed has the same crystal orientation as the substrate.

**Error amplifier**

In voltage regulator circuits, this is the amplifier that takes the error signal, amplifies it, and applies it to the control element.

**Fan-out**

The number of loads connected to the output of a logic stage. (A load normally consists of the input impedance of a logic circuit.)

**Feedforward compensation**

A frequency technique for operational amplifiers that will extend the unity-gain bandwidth and increase the slew rate by high frequency bypassing a frequency limiting stage. For example, the input stage containing lateral P-N-Ps in the signal path.

**Flux density (B)**

The concentration of a magnetic field or magnetic flux in a given unit area.

**Gain error**

When plotting output voltage versus input voltage, the gain of the comparator is the slope of the transfer function of $V_O$ versus $V_{IN}$ while the comparator is in its linear region. The uncertainty of the comparator switching level threshold is called gain error. The higher the gain, the more rectangular the transfer characteristic with a more precise switching level and a smaller gain error.

**Gold doping**

A semiconductor material diffusion doping process used in circuits such as comparators to obtain fast recovery times from saturated transistor switches.

**Ground plane**

A low impedance metal sheet used to minimize ground inductance and shield signal leads.

**Ground shift**

Potential differences that exist between the ground terminals of separate pieces of equipment.

**Harmonic distortion**

Alteration of the original harmonic content of a signal.

**IC driver**

An interface integrated circuit that is used to connect system signals to communicate between low-level system signals and external elements requiring high drive power.

**IC-JFET**

A field-effect transistor formed by diffused junction. The channel is pinched off by applying gate voltage to a diffused junction used as the gate.

**Input loading factor (ILF)**

The ILF is the load that an input line presents to the driver whether the input be to a gate, a board, or a total system. It may be expressed as a current, voltage, impedance, or a combination of these.

**Input offset current ($I_{io}$)**

This is defined as the difference between the separate currents entering a differential input device in the quiescent or balanced state.

**Input offset voltage ($V_{io}$)**

This is the dc voltage that must be applied between an operational amplifier's differential input terminals to force the quiescent dc output voltage to zero.

**Input threshold voltage ($V_{IT}$)**
The comparator input voltage required to produce the output threshold voltage ($V_{OT}$).

**Ion implantation**
A semiconductor fabrication process often used to adjust threshold voltage values in MOS devices by implantation of dopant ions in the gate region after source and drain formation.

**Isolation diffusion**
A p-type diffusion made down through the epitaxial layer to contact p-type substrate and to entirely surround the n-type region of an N-P-N transistor.

**Lateral N-P-N transistor**
A semiconductor device in which the emitter, base, and collector regions are placed side by side in the same horizontal plane.

**Line busy indicator**
An indicator in a transmission line system used in party line systems to indicate the presence of signals on the line, in other words, the line is busy.

**Line driver**
An interface integrated circuit that applies either a constant voltage signal or a constant current signal to a transmission line to send digital data.

**Line receiver**
Basically a threshold detector with a low-level logic compatible output used to receive transmitted digital data.

**Line receiver hysteresis**
The difference between the threshold levels required to switch from a "0" to a "1" output and that required to switch from a "1" to a "0" output level.

**Magnetization force (H)**
Basically the total magnetizing force applied to a material. In a core element, H is a function of the magnitude and direction of the magnetizing current.

**Memory core**
A basic memory storage element consisting of a lithium ferrite core. Magnetization in one direction represents storage of a "one." Magnetization in the opposite direction represents a "zero."

**Modem**

For data transmission, the term is used to refer to the Modulator-Demodulator used as the interface between the system and the transmission media.

**Monolithic integrated circuit**

An electronic circuit consisting of interconnected elements formed in sites on or within a semiconductor substrate with at least one of the elements formed within the substrate.

**MOS capacitor**

A capacitor formed by depositing a dielectric layer over the surface of a conducting semiconductor region within a substrate which forms one electrode. The other electrode is usually a metal layer deposited on top of the dielectric layer.

**MOS transistor (metal-oxide-semiconductor transistor)**

An active semiconductor device in which a conducting channel is induced in the region between two electrodes by a voltage applied to an insulated electrode on the surface of the region.

**MOSFET**

Same as MOS transistor.

**Multiple-collector lateral P-N-P transistor**

An integrated circuit component in which the collector ring in the lateral structure is broken into two sections. The gain of the device can be set very accurately by means of geometry rather than the diffusion characteristics.

**Negative voltage regulator**

A voltage regulator designed specifically to have its control element between the negative supply rail and the negative terminal of the load.

**Noise**

A term referring to spurious or undesirable electrical signals. Noise can be either positive or negative.

**Notch distortion**

This is another name for crossover distortion.

**N-Type semiconductor**

A semiconductor in which electric conduction is due to the presence of more free electrons than holes.

**Offset error**

This is a source of error in determining the comparator's switching threshold level.

**Op amp (operational amplifier)**

A modern op amp is a high gain, direct-coupled amplifier that uses external feedback for control of response characteristics.

**Oscillator**

A special case of a narrowband amplifier in which feedback is used to deliberately cause amplifier instability.

**Output offset voltages**

This is the difference in dc voltage present at two output terminals (or the output terminal and ground for amplifiers with one output) when the input terminals are grounded.

**Output threshold voltage ($V_{OT}$)**

The threshold voltage that the output of a comparator must exceed in order to drive digital circuitry and maintain a specified noise margin.

**Overload recovery time**

This is the time necessary for a control amplifier to regain normal operation after a large signal overload. This is caused by the rectification of strong input signals and the resulting charge on the coupling capacitors.

**Overvoltage protection**

A circuit often used in an integrated circuit to protect against a sudden and/or sustaining high surge voltage.

**Oxidation**

A process that converts the surface of a silicon wafer to silicon dioxide. This is accomplished by subjecting the wafer to oxygen or steam atmosphere at very high temperatures.

**Partial read current ($I_{PR}$)**

Equal to one-half the core read current. This current by itself will not switch a core, but it can be used in conjunction with other currents to aid and switch or to oppose and inhibit the switching of cores.

**Partial write current ($I_{PW}$)**

Equal to one-half the core write current. This current by itself will not switch a core, but it can be used in conjunction with other currents to aid and switch or to oppose and inhibit the switching of cores.

**Party line system**

A transmission system in which the line driver can be transmitting data to more than one receiver at various destinations. Drivers and receivers must be properly synchronized to accomplish this.

**Photomasking**

A semiconductor fabrication process in which a photographic negative is used to delineate selective chemical change to portions of the semiconductor surface.

**Pinch resistor**

A high value, low area resistor used in integrated circuit design whose value depends on an FET biased gate channel.

**Planar transistor**

A diffused-junction transistor in which the emitter, base, and collector regions all come to the same plane surface, with the junctions between the regions protected at the surface by a layer of material such as silicon dioxide.

**P-N junction**

The region of transition between p-type and n-type semiconductor materials.

**Power element drivers**

A group of interface integrated circuit drivers that supply high current to drive electromechanical elements such as printers or relays, or to drive thermal elements such as thermal printers or general purpose heaters.

**Programmable regulators**

IC voltage regulators with a number of sensing resistors contained within the IC for a variety of choices on voltages to be regulated.

**P-Type semiconductor**

A semiconductor in which electric conduction is due to the presence of more holes than free electrons.

**Q of an amplifier**

Q is the ratio of the center frequency, $f_o$, over the bandwidth, B. Q is also referred to as the ratio of energy stored to energy dissipated.

**Random access memory (RAM)**

A memory from which all information can be obtained at the output with approximately the same time delay by choosing an address randomly and without first searching through a vast amount of irrelevant data.

**Read current ($I_R$)**

The value of current through a core to switch the core magnetization to read out the digital data.

**Reference element**

The portion of a voltage regulator circuit responsible for establishing a stable voltage to compare or reference to the sampled output voltage.

**Regulator error signal**

This signal is the voltage difference between a sample of the output voltage and an established reference voltage. The error then activates the corrective regulating elements.

**Residual flux**

The amount of magnetism remaining in a material while not under the influence of a magnetizing force.

**Response time of a comparator**

The delay from the application of the input step until the moment when the output crosses the logic threshold voltage.

**Ripple**

This is used to describe the ac component of a power supply's dc output that has been passed to the output from the ac power source.

**Ripple rejection ratio**

The ratio of the (rms) ac ripple voltage on a voltage regulator output to the ac input voltage (rms).

**Sample-and-hold circuit**

A circuit that performs the operation of looking at a voltage level during a short time period and accurately storing that voltage level for a much longer time period.

**Sampling element**

The circuitry in a voltage regulator that reflects the changes in output voltage which is then compared to the reference element to produce an error signal.

**Schottky-clamped transistor**

A high-speed IC transistor that has a Schottky barrier diode formed parallel to the collector-base junction.

**Schmitt trigger**

A regenerative circuit which changes states abruptly when the input signal crosses specific dc triggering levels.

**Semiconductor**

A material with conductivity roughly midway between that of conductors and insulators, and in which the conductivity increases with temperature over a certain temperature range.

**Semiconductor memory drivers**

Interface integrated circuit drivers used to provide control and timing signals to semiconductor storage elements.

**Sense amplifier**

An integrated circuit amplifier that is an accurate fast threshold detector with a strobing or gating capability and usually with an output that is easily connected to achieve pulse stretching requirements.

**Settling time**

Settling time is the time elapsed from the application of a step function input to the time at which the closed-loop amplifier output has entered and remained within a specified error band around a final value.

**Slew rate**

The average time rate of change of the op amp closed-loop amplifier output voltage for a step-input signal. Slew rate is an important factor affecting accuracy for large signal conditions at high frequency. Normally, slew rate is measured between specified output levels using the largest input voltage step for which amplifier performance remains linear with feedback adjusted for unity gain.

**Substrate**

The physical material on which an integrated circuit is fabricated. Its primary function is mechanical support, but it may serve some electrical function also.

**Super-beta transistor**

An integrated circuit component that has an extra emitter diffusion resulting in a deeper emitter and a correspondingly more narrow base region. Typical super-beta transistors have a gain of several thousand and $B_{BR(CEO)}$ of less than five volts.

**Synchronous demodulator (SD)**

A portion of circuitry designed to operate on a signal that has been chopped and amplified. Its purpose is to demodulate the signal synchronously to return it to its original dc reference and to its time relationship with the high frequency signal portion.

**Temperature coefficient**

The measure of the effect of temperature on a component or a parameter expressed as a rate of change with temperature.

**Totem-pole translator**

This is a commonly used translator that uses a source-sink output stage which makes available translation to any desired positive "1" level and negative "0" level by proper choice of $V_{CC+}$ and $V_{CC-}$ supply levels.

**Transfer function**

The output signal as a function of the input signal through some defined media usually shown in graphical form with the mathematical expression included.

**Transients**

The response of a defined media versus time as a result of an input signal which also is expressed as a response versus time.

**Translator circuit**

Interface integrated circuit between different digital subsystems that converts one set of logic levels to another.

**Truth table**

A chart that tabulates and summarizes all the combinations of possible logic states of the inputs and outputs of a circuit.

**TTL**

Bipolar semiconductor transistor-transistor coupled logic circuits.

**Twisted pair line**

Type of transmission line used between line driver and line receiver consisting basically of two insulated wires twisted together.

**Vertical N-P-N transistor**

A semiconductor device in which the three layers of semiconductor material, N, P and N, form a vertical stack within the substrate.

**Video amplifier**

An amplifier that offers a basic gain element with wide bandwidth usually with a provision for automatic gain control that can be used at all frequencies up to RF range.

**Voltage overdrive**

The excess comparator input voltage beyond that required to bring the output to the threshold voltage. The greater the overdrive, the shorter the response time.

**Voltage regulator**

The voltage regulator is a circuit that has one main function to perform, that of providing an output voltage that is isolated from changes due to input voltage change, output load change, temperature changes and changes with time.

**Write current ($I_W$)**

This is the value of current through a core to cause the core flux to switch states, thereby "writing" in or storing the desired binary state.

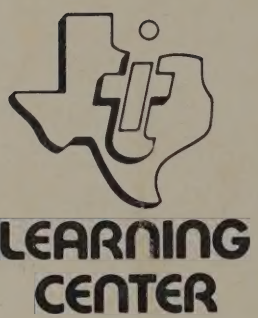
**Zener diode**

A diode that is normally operated in the reverse-biased zener region to provide a relative constant voltage often used as a reference voltage.

**Zero offset voltage**

A characteristic of the ideal op amp such that the output voltage is zero when the input voltage is zero.

# INDEX

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